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Description

BACKGROUND OF THE INVENTION

The present invention is directed to a method of forming thin films of silicon nitrides and other nitrogen-containing compositions, such as oxynitrides, directly on a silicon surface, and is further concerned with the application of such films.

Thin films of silicon nitride have two significant applications in the field of integrated circuits. Since they exhibit a higher dielectric constant and hence a higher unit capacitance than silicon dioxide layers, their use as capacitor dielectrics in small dimension MOS circuits is preferred. The increased unit capacitance that they exhibit make it possible to fabricate capacitors in smaller areas and hence contributes to a denser circuit, relative to a circuit of similar complexity that employs a silicon dioxide film. In addition, silicon nitride films have greater resistance to radiation, alkali ion and other impurity diffusion.

A second application of thin silicon nitride films relates to the electrical isolation of integrated circuits by means of silicon dioxide islands. Typically, these islands are formed by oxidizing selected regions of a silicon substrate. Silicon nitride films are used to protect areas of the substrate where the devices are to be fabricated. In current practice, a thin oxide layer is used between the substrate and a deposited silicon nitride film to prevent the generation of stress-induced faults during oxidation. The presence of this oxide layer permits oxidization to proceed in a lateral, or horizontal, direction as well as in the vertical direction. Oxide encroachment in this lateral direction reduces the area that is subsequently available for fabricating the integrated circuit, and it is therefore preferable to minimize such. Accordingly, attempts have been made to form the thin nitride layer directly on the silicon substrate.

In the past, several different techniques have been employed to form a silicon nitride layer directly on the surface of a silicon substrate. One such technique is the thermal nitridation of silicon, which is carried out using ammonia or nitrogen gases at temperatures in the neighborhood of 1000°C or greater. This approach is disadvantageous in that it requires treatment at high temperatures for extended periods of time and is limited in the types of materials which can be present on or in the substrate. It is particularly unsuitable for use in the fabrication of VLSI devices, since the susceptibility of dopants to diffusion at high temperatures presents problems with the small geometries that are involved. In addition, the resultant films contain a significant amount of oxygen, which hampers their effectiveness in resisting oxidation.

A variation of this technique involves plasma-assisted thermal nitridation with the use of inductively coupled reactors. This technique is disclosed, for example, in U.S. Patent Nos. 4,277,320 and 4,298,629. A coil disposed around the reaction chamber generates an electromagnetic field that inductively heats the wafer to be coated and excites the gas within the chamber to create a plasma. Such reactors have proven to be difficult to construct on a production-scale level, and are therefore not in widespread use. Furthermore, they operate at relatively high temperatures (close to 1000°C) that are produced by the inductive field, and hence have high power requirements.

Another technique for forming thin nitride films uses high energy ion implantation. This technique is generally not desirable from a commercial standpoint, since its throughput is limited by the relatively small ion beam that is employed. In addition, high current implantation systems are complex and expensive.

Low energy ion bombardment is a third technique that has been used to prepare nitride-like films on silicon. Limitations associated with this technique include the fact that processing can only be carried out on a single wafer at a time because of the beam size generated by presently available low energy ion bombardment sources, and the contamination of the resulting layer with materials that are used to fabricate the ion gun source.

A fourth technique for forming silicon nitride films is low pressure chemical vapor deposition (LPCVD). Thickness control of thin films is difficult with this process, and hence the films tend to be relatively thick, in the neighborhood of 300 angstroms or more. As a result, they are not suitable for use in trench isolation when in direct contact with silicon because they can produce stress at the corners of the trench, which leads to defects in adjacent regions of the silicon substrate.

Document JP-A-93242-1983 discloses a method of forming a nitride on a silicon substrate by directly reacting nitrogen containing gas with the surface of the silicon substrate. In a reaction chamber, two parallel flat electrodes are disposed facing oneanother. One of the electrodes carries the wafer and is connected to ground. The other electrode is supplied with r.f. power in the MHz range. Further, the wafer carrying electrode and the wafer itself are heated by means of an induction coil beneath the electrode and fed with r.f. power in the KHz range. The wafer is negatively DC biased. Nitridation takes place at temperatures of about 800°C. Nitride film thicknesses vary between 7 and 15 nm (70 and 150 Angstroms) depending upon the nitridation time of 20 to 90 minutes.

Document J.Appl.Phys. 52(4), 3076 (1981), R. Hezel et al. "Plasma Si nitride - A promising dielectric to

achieve high-quality silicon MIS/IL solar cells" discloses a so-called low temperature plasma-enhanced chemical vapor deposition of silicon nitride. Low temperature, in the context of this document, designates a substrate temperature of 220°C.

The present invention as it is defined by patent claim 1 distinguishes over the former document in that the electrodes have substantially different sizes and that the substrate is cooled such that a temperature of 200°C is not exceeded; preferably, the process is carried out at room temperature. It has been found that under these conditions, the process is self-limiting, i.e. the silicon nitride film thickness ultimately obtained will not increase beyond a certain value upon continued treatment, said value depending upon the applied power.

OBJECTS AND BRIEF STATEMENT OF THE INVENTION

Accordingly, it is an object of the present invention to provide a novel means for economically converting the surfaces of silicon and similar materials into nitride-like layers at relatively low temperatures, i.e. at or near room temperature. In particular, it is an object of the invention to provide a novel method for forming silicon nitride layers, which method does not require an ion gun source and minimizes the energy of ions incident on metallic surfaces, to thereby keep the sputtering and subsequent redeposition of potential contaminants onto the wafer surface low. It is a further object of the invention to provide a novel method of the foregoing type which provides effective control over the thickness of the nitride layer that is formed.

It is a further object of the invention to provide novel applications for thin nitride films.

In accordance with the present invention, these objects are achieved by carrying out a surface reaction on a substrate layer in a vacuum chamber that contains an electrode which is capacitively coupled to an rf generator. A second electrode within the chamber, or a metal wall of the chamber itself, is connected to ground. The silicon wafers to be treated are placed on one of the electrodes to be in electrical and physical contact therewith, and a reagent gas that contains nitrogen is introduced into the chamber. An rf voltage is then applied between the electrodes to create a plasma, causing ions thereof to be accelerated into the silicon substrate. The nitrogen ions that are created as a result of the application of the rf power can be directed at the surface of a number of wafers simultaneously, thereby providing improved throughput over the prior art techniques. In addition, the growth process is self limiting, thereby providing effective control over the thickness of the silicon nitride layer, enabling films that are in the range of 50-100 angstroms thick to be consistently produced.

The thin nitride films that are formed by such a method have a variety of useful applications. Because of their high degree of integrity and high nitrogen-to-oxygen ratio, they are well suited for preventing oxidation during device isolation. Furthermore, the controllability of the thickness of the films readily facilitates the fabrication of capacitors having high unit capacitance. For greater reliability and to reduce leakage currents, the films can be annealed in an oxygen atmosphere when they are to be incorporated in capacitor structures. In addition, the electrical properties of such a film, coupled with its immunity to impurity diffusion and radiation, contribute to its successful application as a gate dielectric for MOSFET devices.

Further features of the invention are described in detail hereinafter with reference to preferred embodiments thereof illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic representation of a chamber of the type that can be used to implement the process of the present invention;

Figures 2 and 3 are cross-sectional views of a silicon wafer during steps of a LOCOS isolation process;

Figure 4 is a cross-sectional view of a trench isolation structure;

Figure 5 is a cross-sectional view of a trench capacitor structure; and

Figure 6 is a cross-sectional view of a MOSFET device incorporating a thin nitride film in the gate dielectric.

DESCRIPTION OF PREFERRED EMBODIMENTS

The method of the present invention for forming a thin film of nitride directly on the surface of a silicon substrate can be carried out in an apparatus of the type illustrated in Figure 1. For example, this apparatus could be a chamber of the type that is typically used for plasma etching. This apparatus basically comprises a sealed metal-walled chamber 10 having a cathode 12 that is electrically insulated from the remainder of the chamber walls, for example by means of a glass insulating ring 14. One wall of the chamber is provided with a loading port 16 to enable silicon wafers to be placed on the cathode 12 and removed therefrom. A vacuum source, such as a turbo-molecular pump 18, is in communication with the chamber to thereby evacuate the same. In addition, the chamber is provided with a gas introduction tube 20 that is connected to a source 22 of

a suitable nitrogen-containing gas through a pressure regulator 24. If appropriate, suitable moisture and oxygen removing cannisters (not shown) can be connected to the tube 20 to improve the purity of the gas that is introduced into the chamber.

The cathode 12 is coupled to an rf generator 26 by means of an in-line capacitor 28, and the metallic walls of the chamber 10 are connected to ground to form an anode. The cathode and the anode thus form a pair of spaced plate electrodes. The generator 26 provides an a.c. current to the cathode at an rf frequency, and the in-line capacitor 28 maintains a d.c. bias on the electrode. Preferably, the area of the anode is much greater than that of the cathode, so that a relatively high self bias, in the range of 300 to 1100 volts, is created at the cathode.

In operation, after the silicon wafers are placed on the cathode 12, and the loading port 16 is closed to seal the chamber, it is evacuated by means of the pump 18 to a low base pressure so as to minimize potentially contaminating residual gases. This base pressure is preferably about 10^{-6} Torr. To effect nitridation, gas from the source 22 is introduced continuously into the evacuated chamber through the tube 20 to maintain the pressure within the chamber at about 10^{-2} Torr. This gas could be pure nitrogen, ammonia or a nitrogen-hydrogen mixture, for example.

The gas within the chamber is activated by applying the power from the rf generator 26 to the cathode. This power can be in the range of about 25 to about 500 watts, and has a frequency of 10 KHz to 300 MHz. As a result of the rf power, a plasma of energized ions of the gas is created. These ions are accelerated into the silicon substrate that is in electrical and physical contact with the cathode, to form a silicon nitride layer.

In order to minimize heating of the silicon wafers as well as prevent cracking of the cathode due to overheating, the cathode can be cooled by any suitable arrangement, such as a water distribution system 30. To inhibit the sputtering of oxygen-containing materials from the glass insulating ring 14 that supports the electrode, a dark space shield 32 can be provided around the electrode. This shield can be made of a suitable conductive material such as aluminum or stainless steel, and can be grounded.

A capacitively coupled rf system such as that illustrated in Figure 1 is capable of creating nitrogen-containing ions of sufficient energy and flux to the surface of the wafer supported on the cathode 12. In contrast to prior systems that employ thermal energy to induce a surface reaction, the system of the present invention utilizes electrically excited nitrogen-containing ions and accelerates them into the silicon surface to promote the chemical reaction. Since the ions can be directed at a relatively large area, a number of wafers can be processed simultaneously, thus making the method of the present invention an economic one for converting the surfaces of silicon into nitride-like layers. In addition, the process is carried out at a relatively low temperature e.g., less than 200°C. (and preferably at room temperature) and does not require an ion gun source.

Furthermore, the process provides inherent control over the thickness of the film that is formed, enabling relatively thin films that are less than 200 angstroms thick, and preferably about 50-100 angstroms thick, to be consistently produced. In particular, the process is self-limiting in that the net growth rate of the nitride film is inversely related to the film's thickness for a given power density. When the film obtains a thickness where its growth rate is equal to the constant rate at which ions sputter off its surface, the process reaches a steady state and no further net growth occurs. For example, for a power density of 0.4 W/cm² of the wafer, the thickness of the film only increases by 5% as the process time is increased from 2 minutes to 45 minutes. By adjusting the power density, films of different desired thicknesses can be obtained.

The control that is afforded by the process described above and the quality of the resulting film facilitate its use in a variety of applications. Through appropriate selection of the density of the applied power (i.e. watts per cm² of the wafer), the atomic nitrogen to nitrogen-plus-oxygen ratio ([N]/[N+O]) of the film can be regulated for a desired application. For example, if the nitride film is to be used to prevent oxidation of selected areas of the wafer during field oxidation, [N]/[N+O] should preferably be at least 90%. When the plasma is formed from N_2, and using an anode:cathode ratio of about 20, powered by a 13.56 MHz rf generator, the [N]/[N+O] ratio can be varied in a range from about 82% (power density = 0.4 W/cm²) to about 98% (power density = 3.2 W/cm²) for 5 minutes. If NH_3 is used to form the plasma, the [N]/[N+O] ratio goes from about 76% to about 96% for the same respective power density settings and time.

Referring to Figures 2 and 3 , one application of the nitride film is illustrated. After a nitride film 36 has been deposited on a silicon substrate 38 in accordance with the method described above, a portion of the film is etched away to define a field region. The portions of the film which remain define the active areas where devices are to be formed. The field regions 40 are oxidized as shown in Figure 3b to provide isolation. The nitride film 36 protects the underlying substrate from oxidation. When the [N]/[N+O] ratio of the film 36 is at least 90%, it has been found that the film will resist more than 4500 angstroms of oxidation.

Subsequent to the formation of the nitride layer, it can be annealed if desired. Such annealing can be carried out by heating the wafer to a temperature between 900 and 1100°C. In order to prevent oxidation of the film, a chamber in which the annealing is carried out can be filled with a non-oxidizing gas such as nitrogen,

hydrogen, or another inert gas. Alternatively, the chamber can be evacuated to achieve the same effect.

Furthermore, the process is not limited to the formation of thin nitride films on planar surfaces. Of particular interest in this context is the formation of the film within trenches. It has been found that high quality thin films can be formed along the side and bottom walls of trench structures in a silicon substrate. Thus, the nitride film can be used as an integral part of the insulating material that fills the trenches for dielectric device isolation.

Referring to Figure 4, a trench 42 is cut into the surface of a silicon wafer to define a boundary between active areas. If desired, the trench could completely surround an active area. The side and bottom walls of the trench are lined with a thin layer 44 of nitride. Preferably, this layer is only 50-70 angstroms thick. The remainder of the trench is then filled with a suitable material 46, such as silicon dioxide or undoped polysilicon. The nitride liner 44 on the walls of the trench acts as a suitable barrier to the diffusion of the material into the silicon substrate.

Advantage can also be taken of the relatively high dielectric permittivity of the film formed according to the above-described process. In particular, silicon nitride has a higher dielectric constant than silicon dioxide. Furthermore, as the thickness of the film is reduced its capacitance increases, so that the relatively thin films that can be obtained with the present invention offer high unit capacitance. To further increase the capacitive applications of nitride films formed according to the process of the invention, they can be annealed in an oxidizing atmosphere to reduce their leakage current.

For example, when used in a dynamic random access memory (DRAM), an integrated capacitor should have high unit capacitance, e.g., at least 5 fF/micron^2, so as to be capable of storing a sufficiently large charge packet that provides immunity to noise. In addition, the capacitor should exhibit low leakage current, e.g. no greater than 10^{-6} A/cm^2 at 2.5 V, so as to afford a refresh cycle time of sufficient duration. The following table illustrates how the properties of a capacitor formed according to the present invention can be improved by annealing it in an oxygen atmosphere. The examples given in the table are with respect to a nitride film formed on a silicon wafer exposed to a plasma created from N_2 gas using an anode:cathode ratio of about 20, powered by a 13.56 MHz rf generator at a power density of 0.4 W/cm^2 for five minutes, in accordance with the above-described process. The oxygen anneal is carried out at 1000°C.

Anneal Time (min)	Capacitance (fF/micron^2)	Leakage Current at 2.5 V (A/cm^2)
0	*	$>10^{-5}$
30	8.8	6×10^{-6}
90	7.7	1.2×10^{-7}

* Not capable of precise measurement due to high leakage current.

As can be seen, the unit capacitance of the film undergoes a slight decrease when annealed, most likely due to its increased thickness and oxygen content as it undergoes oxidation. However, even with an anneal for 90 minutes, the unit capacitance still remains well above the minimum noted previously for DRAM applications, whereas the leakage current is reduced by two orders of magnitude over a film which has not been annealed.

The annealing temperature and time can be shortened, for example by utilizing steam at 900°C for 10-15 minutes. As another alternative, it is possible to employ a rapid thermal anneal (RTA) in which high temperatures are applied to the wafer for very short periods of time, e.g., tens of seconds. It is believed that results which are equivalent to or better than those depicted above can be obtained with these alternative annealing processes.

Due to the ability of the inventive process to produce high-quality nitride films within trenches, it becomes possible to fabricate trench capacitor structures. Such a structure is illustrated in Figure 5. The capacitor basically comprises a thin nitride film 48 formed along the upper surface and within a trench formed in an appropriately doped layer 50 of silicon or polysilicon. The layer 50 functions as one electrode of the capacitor, and a second electrode 52 is formed by depositing a metal or doped polysilicon over the nitride layer 48. If the trench has a width W and a depth D, its capacitance would be (1 + 4D/W) times greater than that of a capacitor formed on top of layer 50 and occupying the same amount of surface area.

Another particularly useful application for nitride films formed according to the process of the present in-

vention is as a gate dielectric for MOSFET devices. In the past, attempts at constructing a MOSFET using a thin oxide film in the gate region and a doped polysilicon for the gate conductor have met with several limitations. One of these limitations has been with respect to the impurity that is used to dope the polysilicon. Boron would be a desirable dopant for the polysilicon layer to produce an enhancement type MOSFET. However, the diffusion coefficient for boron is enhanced in the presence of hydrogen during the deposition of polysilicon. Consequently, it tends to break through the oxide layer and dope the underlying channel region. Phosphorous dopant would be another possibility but it suffers from the fact that it would create a depletion type of n-channel MOSFET.

However, by using a nitride film as the gate dielectric, the tendency of boron to diffuse into the channel region is resisted. Furthermore, even though the interface state density of the nitride film is higher than that of silicon dioxide layers, the nitride's contribution to the threshold voltage of the device is minimal, due to its small thickness and high permittivity. Therefore, it is possible to produce enhancement type MOSFETS of higher reliability and integrity using a combination of the above-mentioned features.

Such a device is illustrated in Figure 6. The device comprises a channel region 54 of silicon that is doped to one conductivity, e.g. n-type. Source and drain regions 56 of opposite conductivity are located on opposite sides of the channel region. A thin film of silicon nitride 58 is grown over the channel region to provide the gate dielectric. A silicon dioxide layer 60 covers the remaining portion of the surface of the substrate, and suitable contact holes 62 are provided for the source and drain electrodes. A thin layer of silicon dioxide 64 can also be disposed over the nitride film. In fact, the interface between the nitride layer 58 and the silicon dioxide layer 64 may not be well-defined, but rather comprise a blend from primarily nitride to primarily oxide over a distance of 5-20 angstroms. A polysilicon layer 66 that is doped with boron is deposited over the thin gate dielectric films 58 and 64 to form the gate electrode.

In summary, the nitride films that are produced according to the process of the present invention have at least two significant areas of application, as barriers for isolation and during oxidation, and as elements of electrical devices such as capacitors and MOSFETS. In the former area of application, it is desirable that the film have a high purity, i.e., [N]/[N+O] is high. Accordingly, the process should be carried out at relatively high power density levels, e.g., 1.6-3.2 W/cm^2, and at relatively low pressures. For electrical applications, where the film is preferably annealed in oxygen, its purity is not so much a factor as its electrical characteristics. Accordingly, the process can be carried out with lower power densities, for example in the range of 0.4-2.0 W/cm^2. Further in this regard, films made with N_2 as the source appear to be best suited for use as gate dielectrics, whereas those made with NH_3 are preferred for use in capacitors since they exhibit higher unit capacitance for a given leakage current.

Claims

1. A method of preparing a thin film of silicon nitride or other nitrogen-containing composition on a silicon substrate, in a capacitively coupled plasma deposition chamber with parallel electrodes comprising the steps of:

   placing one surface of silicon substrate in contact with a first of a pair of plate electrodes, said first electrode being spaced away and opposite from a second plate electrode of said pair of electrodes which faces the opposite surface of said substrate and has an area greater than said first of said pair of electrodes;

   evacuating a chamber in which said electrodes and the substrate are located;

   introducing a nitrogen-containing reagent gas free of silicon compounds into the space between said pair of electrodes; and

   applying an a.c. voltage having a frequency of about 10 KHz or greater between said electrodes to thereby ionize and activate the reagent gas and accelerate ions thereof into the substrate while cooling said first of said pair of electrodes to inhibit heating of said substrate wherein the temperature of said substrate is less than 200°C.

2. The method of claim 1 wherein said reagent gas comprises one of pure nitrogen, ammonia and a nitrogen-hydrogen mixture.

3. The method of claim 1 further including the step of annealing the thin film of nitride formed on said substrate.

4. The method of claim 3 wherein said annealing step is carried out in the presence of a non-oxidizing gas.

5. The method of claim 1 wherein the area of the other electrode of said pair of electrodes is at least twice as great as the area of said one electrode.

6. The method of one of the preceding claims for isolating active regions from one another in an integrated circuit, comprising the steps of:

removing selected portions of said film so that the remaining portions of the film correspond to areas in which active devices are to be formed in the wafer; and

oxidizing the areas on said surface of the wafer that are not covered by the remaining portions of the nitride film.

7. The method of claim 6 wherein said a.c. voltage signal has a power density in the range of about 1.6 to about 3.2 W/cm^2 of the substrate.

8. The method of claim 6 wherein said nitride film has a thickness no greater than 20 nm (200 angstroms).

9. The method of claim 8 wherein said film has a thickness in the range of about 5 to about 10 nm (50 to about 100 angstroms).

10. The method of claim 6 wherein the ratio of nitrogen to nitrogen-plus-oxygen in said film is at least 90%.

11. The method of claim 6 wherein the pressure of said plasma is about 10^{-2} Torr.

12. The method of claim 6 wherein said opposite surface of the substrate has a trench in it, and said nitride film remains in the trench after said selective removing step.

13. The method of one of claims 1 to 5 for dielectrically isolating active regions from one another in an integrated circuit, comprising the steps of:

forming a trench in the exposed surface of said substrate to define a boundary of at least one area in which an active device is to be located; and after said nitride film is formed on said surface of the substrate and along the walls of said trench:

filling the remainder of said trench with an insulating material.

14. The method of claim 13 wherein said film has a thickness of about 5 to about 7 nm (50 to about 70 angstroms).

15. The method of claim 13 wherein said a.c. voltage signal has a power density in the range of about 1.6 to about 3.2 W/cm^2 on the substrate.

16. The method of claim 13 wherein the ratio of nitrogen to nitrogen-plus-oxygen in said film is at least 90%.

17. The method of claims 1, 2, and 3 wherein said a.c. voltage signal has a power density of about 0.4 to about 2.0 W/cm^2 of the substrate.

18. The method of claim 17 further including the step of depositing an electrode on the surface of said nitride film that is opposite the silicon to thereby form a capacitor.

19. The method of claim 18 wherein said nitride film comprises the gate dielectric for a MOSFET, and further including the step of depositing a doped polysilicon on said film to form the gate electrode of the MOSFET.

20. The method of claim 19 wherein said polysilicon is doped with boron.

21. The method of claim 19 further including the step of forming a thin layer of oxide between said nitride film and said polysilicon gate electrode.

22. The method of claim 3 wherein said annealing is carried out in the presence of oxygen.

Patentansprüche

1. Ein Verfahren zum Bilden einer dünnen Schicht von Siliciumnitrid oder einer anderen Stickstoff enthaltenden Zusammensetzung auf einem Siliciumsubstrat in einer kapazitiv gekoppelten Plasmaauftragkammer mit parallelen Elektroden, umfassend die Schritte:

Plazieren einer Oberfläche des Siliciumsubstrats in Kontakt mit einer ersten eines Paares von Plattenelektroden, welche erste Elektrode von einer zweiten Plattenelektrode des Paares von Elektroden beabstandet ist und dieser gegenüberliegt, welche der entgegengesetzten Oberfläche des Substrats zugewandt ist und eine Fläche aufweist, die größer ist als die erste des Paares von Elektroden;

Evakuieren einer Kammer, in der sich die Elektroden und das Substrat befinden;

Einspeisen eines Stickkstoff enthaltenden Reagenzgases, das frei von Siliciumverbindungen ist, in den Raum zwischen dem Paar von Elektroden,; und

Anlegen einer Wechselspannung mit einer Frequenz von etwa 10 KHz oder größer zwischen den Elektroden, um dadurch das Reagenzgas zu ionisieren und aktivieren und Ionen desselben in das Substrat zu beschleunigen, während die erste des Paares von Elektroden gekühlt wird, um das Aufheizen des Substrats zu unterbinden, wobei die Temperatur des Substrats bei weniger als 200°C liegt.

2. Das Verfahren nach Anspruch 1, bei dem das Reagenzgas eines von reinem Stickstoff, Ammonium und einem Stickstoff-Wasserstoff-Gemisch umfaßt.

3. Das Verfahren nach Anspruch 1, ferner umfassend den Schritt des Anlassens der dünnen Schicht aus Nitrid, die auf dem Substrat gebildet worden ist.

4. Das Verfahren nach Anspruch 3, bei dem der Anlaßschritt in Gegenwart eines nichtoxidierenden Gases ausgeführt wird.

5. Das Verfahren nach Anspruch 1, bei dem die Fläche der anderen Elektrode des Paares von Elektroden mindestens zweimal so groß ist wie die Fläche der einen Elektrode.

6. Das Verfahren nach einem der vorangehenden Ansprüche für das Isolieren von aktiven Bereichen von einander in einem integrierten Schaltkreis, umfassend die Schritte:

Abtragen ausgewähler Abschnitte der Schicht so, daß die verbleibenden Abschnitte der Schicht den Flächen entsprechen, in welchen aktive Komponenten in dem Wafer zu bilden sind; und

Oxidieren der Bereiche auf der Oberfläche des Wafers, die nicht von den verbleibenden Abschnitten der Nitridschicht abgedeckt sind.

7. Das Verfahren nach Anspruch 6, bei dem das Wechselspannungssignal eine Leistungsdichte im Bereich von etwa 1,6 bis etwa 3,2 W/cm^2 des Substrats hat.

8. Das Verfahren nach Anspruch 6, bei dem die Nitridschicht eine Dicke von nicht mehr als 20 nm (200 Å) hat.

9. Das Verfahren nach Anspruch 8, bei dem die Schicht eine Dicke im Bereich von etwa 5 bis etwa 10 nm (50 - etwa 100 Å) hat.

10. Das Verfahren nach Anspruch 6, bei dem das Verhältnis von Stickstoff zu Stickstoff-plus-Sauerstoff in der Schicht mindestens 90% beträgt.

11. Das Verfahren nach Anspruch 6, bei dem der Druck des Plasmas etwa 10^{-2} Torr beträgt.

12. Das Verfahren nach Anspruch 6, bei dem die gegenüberliegende Oberfläche des Substrats einen Graben aufweist und die Nitridschicht in dem Graben nach dem selektiven Abtragschritt verbleibt.

13. Das Verfahren nach einem der Ansprüche 1 bis 5 für die dielektrische Isolation aktiver Bereiche voneinander in einem integrierten Schaltkreis, umfassend die Schritte:

Bilden eines Grabens in der exponierten Oberfläche des Substrats zum Definieren einer Grenze mindestens eines Bereichs, in welchem eine aktive Komponente zu positionieren ist; und, nachdem die Nitridschicht auf der Oberfläche des Substrats und längs der Wandungen des Grabens gebildet worden

ist,

Füllen des Restes des Grabens mit einem isolierenden Material.

14. Das Verfahren nach Anspruch 13, bei dem die Schicht eine Dicke von etwa 5 bis etwa 7 nm (50 bis etwa 70 Å) hat.

15. Das Verfahren nach Anspruch 13, bei dem das Wechselspannungssignal eine Leistungsdichte im Bereich von etwa 1,6 bis etwa 3,2 W/cm² auf dem Substrat hat.

16. Das Verfahren nach Anspruch 13, bei dem das Verhältnis von Stickstoff zu Stickstoff-plus-Sauerstoff in der Schicht mindestens 90% beträgt.

17. Das Verfahren nach Ansprüchen 1, 2 und 3, bei dem das Wechselspannungssignal eine Leistungsdichte von etwa 0,4 bis etwa 2,0 W/cm² des Sustrats hat.

18. Das Verfahren nach Anspruch 17, ferner umfassend den Schritt des Aufbringens einer Elektrode auf der Oberfläche der Nitridschicht, die dem Silicium abgekehrt ist, um dadurch einen Kondensator zu bilden.

19. Das Verfahren nach Anspruch 18, bei dem die Nitridschicht das Gate-Dielektrikum für einen MOSFET umfaßt, und ferner umfassend den Schritt des Aufbringens eines dotierten Polysiliciums auf die Schicht zur Bildung der Gate-Elektrode des MOSFET.

20. Das Verfahren nach Anspruch 19, bei dem das Polysilicium mit Bor dotiert ist.

21. Das Verfahren nach Anspruch 19, ferner umfassend den Schritt der Bildung einer dünnen Schicht aus Oxid zwischen der Nitridschicht und der Polysilicium-Gate-Elektrode.

22. Das Verfahren nach Anspruch 3, bei dem das Anlassen in Gegenwart von Sauerstoff ausgeführt wird.

Revendications

1. Procédé pour la préparation d'un film mince de nitrure de silicium ou d'une autre composition contenant de l'azote sur un substrat en silicium, dans une chambre de dépôt par plasma à électrodes parallèles couplée de façon capacitive comprenant les étapes consistant à :

disposer une surface du substrat en silicium en contact avec une première électrode d'une paire d'électrodes en plaque, ladite première électrode étant espacée et en regard d'une deuxième électrode en plaque de ladite paire d'électrodes qui est en regard de la surface opposée dudit substrat et a une surface supérieure à ladite première électrode de ladite paire d'électrodes;

créer un vide dans une chambre dans laquelle lesdites électrodes et le substrat sont disposés;

introduire un gaz réactif contenant de l'azote et ne comprenant pas de composés de silicium dans l'espace situé entre ladite paire d'électrodes; et

appliquer une tension alternative ayant une fréquence d'environ 10 KHz ou plus entre lesdites électrodes pour ainsi ioniser et activer le gaz réactif et accélérer ses ions dans le substrat tout en refroidissant ladite première électrode de ladite paire d'électrodes pour empêcher le chauffage dudit substrat, la température dudit substrat étant inférieure à 200°C.

2. Procédé selon la revendication 1 dans lequel ledit gaz réactif comprend de l'azote pur, de l'ammoniac ou un mélange d'azote et d'hydrogène.

3. Procédé selon la revendication 1 comprenant en outre l'étape de recuire le film mince de nitrure formé sur ledit substrat.

4. Procédé selon la revendication 3 dans lequel ladite étape de recuit est réalisée en présence d'un gaz non-oxydant.

5. Procédé selon la revendication 1 dans lequel la surface de l'autre électrode de ladite paire d'électrodes est au moins deux fois plus grande que la surface de ladite première électrode.

6. Procédé selon l'une des revendications précédentes pour isoler des régions actives les unes des autres dans un circuit intégré, comprenant les étapes consistant à :

enlever des parties sélectionnées dudit film de sorte que les parties restantes du film correspondent à des surfaces dans lesquelles des dispositifs actifs doivent être formés dans la plaquette; et

oxyder les surfaces sur ladite surface de la plaquette qui ne sont pas couvertes par les parties restantes du film de nitrure.

7. Procédé selon la revendication 6 dans lequel le signal de tension alternative a une densité de puissance comprise dans la gamme d'environ 1,6 à 3,2 W/cm^2 du substrat.

8. Procédé selon la revendication 6 dans lequel le nitrure a une épaisseur qui n'est pas supérieure à 20 nm (200 angströms).

9. Procédé selon la revendication 8 dans lequel ledit film a une épaisseur comprise dans la gamme d'environ 5 à environ 10 nm (50 à environ 100 angströms).

10. Procédé selon la revendication 6 dans lequel le rapport entre l'azote et l'azote plus l'oxygène dans ledit film est d'au moins 90%.

11. Procédé selon la revendication 6 dans lequel la pression dudit plasma est d'environ 10^{-2} Torr.

12. Procédé selon la revendication 6 dans lequel ladite surface opposée du substrat comprend une tranchée et ledit film de nitrure reste dans la tranchée après ladite étape d'élimination sélective.

13. Procédé selon l'une des revendications 1 à 5 pour isoler de façon diélectrique des régions actives les unes des autres dans un circuit intégré, comprenant les étapes consistant à :

former une tranchée dans la surface exposée dudit substrat pour définir une limite d'au moins une zone dans laquelle un dispositif actif doit être disposé; et après que le film de nitrure a été formé sur ladite surface du substrat et le long des parois de ladite tranchée :

remplir le reste de ladite tranchée avec un matériau isolant.

14. Procédé selon la revendication 13 dans lequel ledit film a une épaisseur d'environ 5 à environ 7 nm (50 à environ 70 angströms).

15. Procédé selon la revendication 13 dans lequel ledit signal de tension alternative a une densité de puissance comprise dans la gamme d'environ 1,6 à environ 3,2 W/cm^2 sur le substrat.

16. Procédé selon la revendication 13 dans lequel le rapport d'azote à l'azote plus l'oxygène dans ledit film est d'au moins de 90%.

17. Procédé selon les revendications 1, 2 et 3 dans lequel ledit signal de tension alternative à une densité de puissance d'environ 0,4 à environ 2,0 W/cm^2 du substrat.

18. Procédé selon la revendication 17 comprenant en outre l'étape consistant à déposer une électrode sur la surface dudit film de nitrure qui est opposée au silicium pour former ainsi un condensateur.

19. Procédé selon la revendication 18 dans lequel ledit film de nitrure comprend un diélectrique de grille pour un MOSFET, et comprend en outre l'étape consistant à déposer un polysilicium dopé sur ledit film pour former l'électrode de grille du MOSFET.

20. Procédé selon la revendication 19 dans lequel ledit polysilicium est dopé avec du bore.

21. Procédé selon la revendication 19 comprenant en outre l'étape consistant à former une couche mince d'oxyde entre ledit film de nitrure et ladite électrode de grille en polysilicium.

22. Procédé selon la revendication 3 dans lequel le recuit est réalisé en présence d'oxygène.

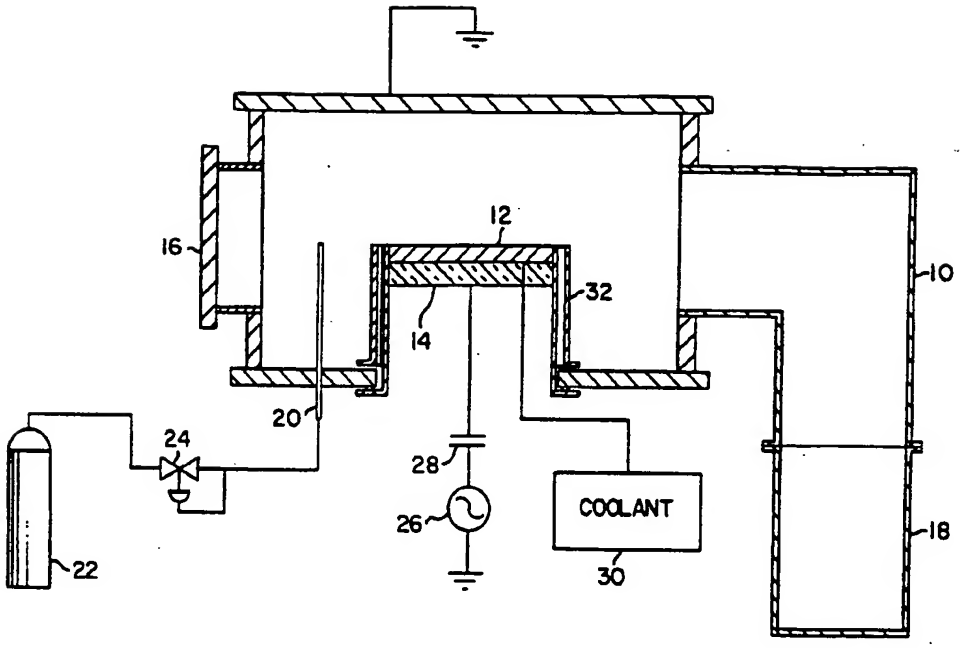

FIG.1

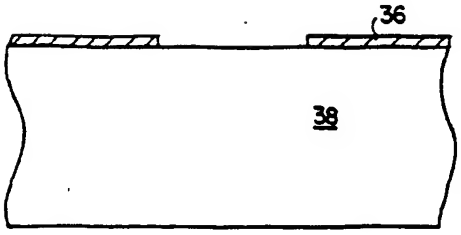

FIG. 2

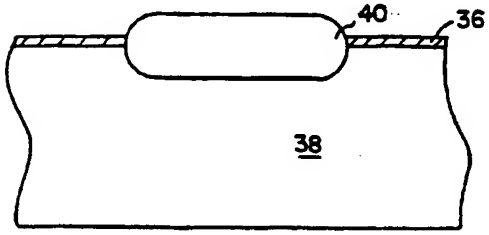

FIG. 3

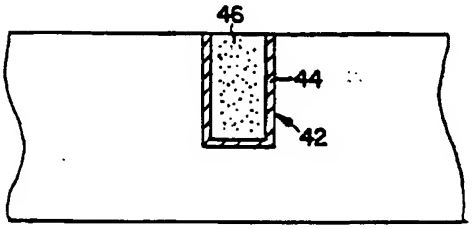

FIG. 4

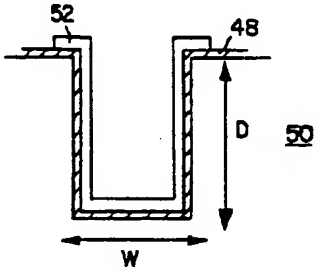

FIG. 5

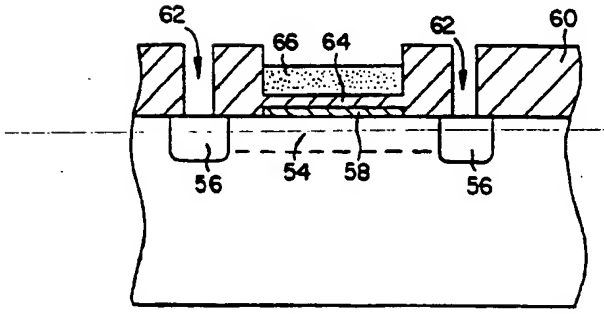

FIG. 6

Third-Party Search Results

Citations from Dissertation Abstracts: DIS

1. NDN 135-0097-1501-6: MULTILEVEL INTERCONNECTION TECHNOLOGIES--A FRAMEWORK AND EXAMPLES

Citations from Energy Database: EDB

2. NDN 108-0539-1134-4: Electrophysical investigation of thin-layered inorganic coatings

Citations from Energy Database: ED1

3. NDN 168-0400-4358-5: Microelectronic thin film deposition by ultraviolet laser photolysis
MONOGRAPH TITLE- Laser processing of semiconductor devices

Citations from European Fulltext Granted Patents: EFB

4. NDN 080-0136-2848-4: Method of producing a CMOS inverter on a soi-substrate with a SIMOX technique PATENT NUMBER- 0554063/EP-B1

5. NDN 080-0135-8224-4: Method of enhancing the withstand voltage of a multilayered semiconductor device PATENT NUMBER- 0419898/EP-B1

6. NDN 080-0089-3105-9: PROCESS FOR MANIPULATING MICROSCOPICALLY SMALL DIELECTRIC PARTICLES AND DEVICE FOR IMPLEMENTING THE PROCESS PATENT NUMBER- 0555252/EP-B1

7. NDN 080-0087-3408-1: SEMICONDUCTOR FILM BOLOMETER THERMAL INFRARED DETECTOR PATENT NUMBER- 0526551/EP-B1

8. NDN 080-0086-8425-2: Process for cleaning oxidized metallic surfaces in the fabrication of interconnection networks and boards for such networks PATENT NUMBER- 0518774/EP-B1

9. NDN 080-0085-8741-4: Heat treatment of Si single crystal PATENT NUMBER- 0503816/EP-B1

10. NDN 080-0084-8883-7: Method for testing electrical properties of silicon single crystal PATENT NUMBER- 0487302/EP-B1

11. NDN 080-0064-9017-3: Low temperature plasma nitridation process and applications of nitride films formed thereby PATENT NUMBER- 0201380/EP-B1

12. NDN 080-0061-2955-7: In situ monitoring technique and apparatus for chemical/mechanical planarization endpoint detection PATENT NUMBER- 0455455/EP-B1

13. NDN 080-0020-9005-0: A programmable element for a semiconductor integrated circuit chip PATENT NUMBER- 0224418/EP-B1

Citations from Engineering Index: EI1

14. NDN 017-0162-4540-3: Surface micromachined pressure transducers.

Citations from Engineering Index: EI2

15. NDN 163-0241-9685-5: Measurement of polyimide interlayer adhesion using microfabricated structures.

Citations from INSPEC: IN2

16. NDN 083-0456-5984-0: Residual stress in PZT thin films and its effect on ferroelectric properties

17. NDN 083-0401-5570-3: Stress and stress relaxation in integrated circuit metals and dielectrics

18. NDN 083-0400-0730-0: Properties of a photoimageable thin polyimide film

19. NDN 083-0374-3142-2: Control of thin film materials properties used in high density multichip interconnect

Citations from INSPEC (80-89): IN3

20. NDN 161-0331-2580-8: Metalized MIC substrates using high K dielectric resonator materials

21. NDN 161-0327-9154-3: Stresses in borophosphosilicate glass films during thermal cycling

22. NDN 161-0327-9151-9: Low stress films of cyclized polybutadiene dielectrics by vacuum annealing

23. NDN 161-0325-2065-2: Passivation of GaAs FET's with PECVD silicon nitride films of different stress states

24. NDN 161-0321-3789-5: Characterization of a spin-applied dielectric for use in multilevel metallization

25. NDN 161-0311-1185-9: Material characteristics of spin-on glasses for interlayer dielectric applications

26. NDN 161-0275-3176-3: Stress measurements on multilevel thin film dielectric layers used in Si integrated circuits

27. NDN 161-0212-7483-2: Laser photolytic deposition of thin films

28. NDN 161-0201-7251-6: Low temperature double-exposed polyimide/oxide dielectric for VLSI multilevel metal interconnection

Citations from INSPEC (69-79): IN4

29. NDN 082-0050-6162-5: A switching plate with aluminium membrane crossings of conductors

30. NDN 082-0050-5840-7: Internal stresses and resistivity of low-voltage sputtered tungsten films (microelectronic cct. conductor)

31. NDN 082-0039-2832-0: An evaluation of methods for passivating silicon integrated circuits

Citations from WORLD PATENT FULLTEXT: PC2

32. NDN 052-0140-0809-9: MULTICHIP INTEGRATED CIRCUIT MODULE AND METHOD OF FABRICATION, -1992017901/WO-A1/ PUBLICATION NUMBER- 1992017901/WO-A1

33. NDN 052-0124-5626-6: EXTENDED INTEGRATION SEMICONDUCTOR STRUCTURE AND METHOD OF MAKING THE SAME, -1990009093/WO-A1/ PUBLICATION NUMBER- 1990009093/WO-A1

34. NDN 052-0120-6199-1: REDUCING STEREOLITHOGRAPHIC PART DISTORTION THROUGH ISOLATION OF STRESS, -1989010255/WO-A1/ PUBLICATION NUMBER- 1989010255/WO-A1

Citations from US PATENT FULLTEXT: US2

35. NDN 064-2592-7787-5: Method of forming patterned polyimide films PATENT NUMBER- 05470693

36. NDN 064-2519-6676-4: Global planarization process PATENT NUMBER- 05284804

37. NDN 064-2446-9512-4: Avoiding spin-on-glass cracking in high aspect ratio cavities PATENT NUMBER- 05119164

38. NDN 064-2405-8655-8: Method for coplanar integration of semiconductor ic devices PATENT NUMBER- 04990462

39. NDN 064-2381-4169-7: Electro-optic signal measurement PATENT NUMBER- 04928058

Citations from US PATENT FULLTEXT: US3

40. NDN 067-2264-7934-2: Formation and planarization of silicon-on-insulator structures PATENT NUMBER- 04604162

Citations from US PATENT FULLTEXT: US5

41. NDN 196-2443-9436-3: Incorporation of dielectric layers in a semiconductor

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Citations from Dissertation Abstracts: DIS

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1. MULTILEVEL INTERCONNECTION TECHNOLOGIES--A FRAMEWORK AND

EXAMPLES
DIS 93-18-BK AAI8814014 NDN- 135-0097-1501-6

AUTHORS- PAI, PEI-LIN
Chairman: WILLIAM G. OLDHAM
VOLUME 49-05B
PUBLICATION DATE- 1987
PP 1871
146 PAGES
CORPORATE AUTHOR- UNIVERSITY OF CALIFORNIA, BERKELEY
INSTITUTION CODE- 0028
Degree- PH.D.
SUBFILE CODE- DAI
Document Order Number- AAI8814014
Section- The Sciences and Engineering
LANGUAGE- English (DEF)
Multilevel interconnection is widely practiced today; however, the difficulties in the metal patterning and topography planarization processes motivate more research in interconnection technology. An additive thin-film patterning process (LOPED) is examined, and a planarization process using spin-on glass is investigated. The metallization process in general is studied, and those approaches that can be extended beyond VLSI are selected for more detailed study. I. Thin-film patterning. A new lift-off process using edge-detection (LOPED) can pattern thin films deposited with good step coverage. Some guidelines, including a process window, have been developed for the LOPED process to assure successful patterning. The potential of this process is demonstrated for both metallization and trench isolation. In the lifting step of the LOPED process, acetone penetrates into the patterning resist with a constant speed, leaving a swollen region behind a sharp boundary. The penetration velocity is related to the metal deposition time and volume increase. II. Planarization. Both the current planarization processes using spin-on glass (SOG) are severely challenged when the underlying metal pitch approaches 2.5\mum unless a sandwich structure (SOG/LTO/SOG) is used. The material properties needed for successful applications of SOG are investigated. Infrared spectrophotometry shows that the concentration of hydroxyl and organic groups are sensitive to the annealing conditions. The stress levels of SOG films on Si wafers are always low (less than 10\sp8Pa in tensile). A strong correlation between the dielectric properties and the OH content in the film is established. SOG IC1-200 (Futurrex Company) shows low dielectric constants and high breakdown fields after 400\sp\circC annealing. III. Metallization framework. A general examination of the metallization process shows that, under some practical assumptions, there are thirteen ways to construct a metallization process. Out of the thirteen ways, six do not require planarization after interconnect patterning and are considered promising for VLSI and beyond. Selective metal deposition, e.g. electroless plating, is required by all six approaches. Electroless-plated Ni and Pd may be used for via filling and Cu for interconnects. A buried metal process, either using lift-off or electroless plating, can provide a planarized surface after metallization.
DESCRIPTOR- ENGINEERING, ELECTRONICS AND ELECTRICAL
SECTIONAL CLASSIFICATION CODE- 0544 .

Citations from Energy Database: EDB

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2. Electrophysical investigation of thin-layered inorganic coatings
EDB 91-06 91:034254 91000413221 NDN- 108-0539-1134-4

AUTHORS- Kochugova, I. V.; Nikolaeva, L. V.; Vakser, N. M., (M.I. Kalinin Leningrad Polytechnic Institute (USSR))
JOURNAL NAME- Inorganic Materials (English Translation) (USA)
ABBREVIATED JOURNAL TITLE- Inorg. Mater. (Engl. Transl.)
VOLUME 25
NUMBER 6
PUBLICATION DATE- 1989-11
PP 826-828
DOCUMENT TYPE- Journal Article
ISSN- 0020-1685
CODEN- INOMA
AUTHOR AFFILIATION- M.I. Kalinin Leningrad Polytechnic Institute (USSR)
LOCATION OF WORK- SU
LITERARY INDICATOR- Translation
TRANSLATION INFORMATION- Translation of Izvestiya Akademii Nauk SSSR, Neorganicheskie Materialy; 25: No. 6, 981-983(Jun 1989)
SUBFILE CODE- JMT
PUBLICATION COUNTRY- US
ANNOUNCEMENT CODE- EDB; ETD
INCOMING TAPE SERIAL NUMBER- JT9059%%545
ANNOUNCEMENT IDENTIFICATION- EDB-91:034254
LANGUAGE- English
The electrical resistivity of compositions can be raised by creation of coatings based on glassy binder and highly dispersed fillers. To this end, gelatinous solutions containing 40-65% of tetraethylorthosilicate (TEOS) as the glass-forming component and aqueous salt solutions as well as solutions containing orthophosphoric acid instead of TEOS as the glass-forming component are used. In this work, inorganic coatings (IC) which are prepared from suspensions consisting of powdered filler (50-60 mass %) distributed in a dispersing medium, a solution which forms a glassy-matrix coating upon firing, are studied. Inorganic coatings placed on a metal base as a thin layer (20-25 mu m) combine good electrical insulating properties with pliability and elasticity. The dielectric losses in the compositions studied are defined by conductivity and polarization. They grow with heating. The properties of the coatings, prepared from a suspension of filler in a glass-forming solution, depend mainly on the nature of filler and can change substantially with exchange of one filler by another.
DESCRIPTOR- *ALUMINIUM OXIDES --Electrical properties; *CHROMIUM OXIDES --Electrical properties; *COATINGS --Electrical properties; *ELECTRICAL INSULATION --Electrical properties ACETATES; ALUMINIUM; BINDERS; CAPACITANCE; DIELECTRIC PROPERTIES; DISPERSIONS; ELASTICITY; ELECTRIC CONDUCTIVITY; ELECTRIC CONDUCTORS; FILLERS; GLASS; LOSSES; MATRIX MATERIALS; NICHROME; NICKEL; NITRATES; STAINLESS STEELS; SUBSTRATES; TEMPERATURE DEPENDENCE; THIN FILMS IDENTIFIER- ALLOY-NI60FE24CR16; ALLOYS; ALUMINIUM COMPOUNDS; CARBOXYLIC ACID SALTS; CHALCOGENIDES; CHROMEL; CHROMIUM ALLOYS; CHROMIUM COMPOUNDS; CORROSION RESISTANT ALLOYS; ELECTRICAL PROPERTIES; ELEMENTS; FILMS; HEAT RESISTANT MATERIALS; HEAT RESISTING ALLOYS; HIGH ALLOY STEELS; IRON ALLOYS; IRON BASE ALLOYS; MATERIALS; MECHANICAL PROPERTIES; METALS; NICKEL ALLOYS; NICKEL BASE ALLOYS; NITROGEN COMPOUNDS; OXIDES; OXYGEN COMPOUNDS; PHYSICAL

PROPERTIES; STEELS; TENSILE PROPERTIES; TRANSITION ELEMENT COMPOUNDS; TRANSITION ELEMENTS
SECTIONAL CLASSIFICATION CODE- 360204

Citations from Energy Database: ED1

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3. Microelectronic thin film deposition by ultraviolet laser photolysis
MONOGRAPH TITLE- Laser processing of semiconductor devices
EDB 85-01 85:004392 8411524969 NDN- 168-0400-4358-5

AUTHORS- Boyer, P. K.; Collins, G. J.; Moore, C. A.; Ritchie, W. K.; Roche, G. A.; Solanski, R.(A); Tang, C. C.(M)
PUBLICATION DATE- 1983
120-126 PAGES
DOCUMENT TYPE- Book Analytic
AUTHOR AFFILIATION- Colorado State Univ., Fort Collins, CO
LOCATION OF WORK- US
LITERARY INDICATOR- Conference
REPORT NUMBER- CONF-830123--
PUBLISHER- SPIE
PUBLICATION PLACE- Bellingham, WA, USA
PUBLICATION COUNTRY- US
CONFERENCE DATE- 24 Jan 1983
CONFERENCE TITLE- International Society for Optical Engineering (SPIE) conference

CONFERENCE LOCATION- Los Angeles, CA, USA
ANNOUNCEMENT CODE- INS; EDB
ANNOUNCEMENT IDENTIFICATION- EDB-85:004392
ORIGINAL SERIAL TITLE- Proceedings of the SPIE, vol. 385
An excimer laser is used to photochemically deposit thin films of silicon dioxide, silicon nitride, aluminum oxide, and zinc oxide at low temperatures (100-350 sup 0 C). Deposition rates in excess of 3000 A/min and conformal coverage over vertical walled steps were demonstrated. The films exhibit low defect density and high breakdown voltage and have been characterized using IR spectrophotometry, AES, and C-V analysis. Device compatibility has been studied by using photodeposited films as interlayer dielectrics, diffusion masks, and passivation layers in production CMOS devices. Additionally, the authors deposited metallic films of Al, Mo, W, and Cr over large (>5 cm sup 2) areas using UV photodissociation of trimethylaluminum and the refractory metal hexacarbonyls. Both shiny metallic films as well as black particulate films were obtained depending on the deposition geometry. The black films are shown to grow in columnar grains. The depositions were made at room temperature over pyrex and quartz plates as well as silicon wafers. They examined the resistivity, adhesion, stress and step coverage of these films. The films exhibited resistivities at most about20 times that of the bulk materials and tensile stress no higher than 7 x 10 sup 9 dynes/cm sup 2 .
DESCRIPTOR- *ALUMINIUM OXIDES --Deposition; *ALUMINIUM OXIDES --Photolysis; *SILICON NITRIDES --Deposition; *SILICON NITRIDES --Photolysis; *SILICON OXIDES --Deposition; *SILICON OXIDES --Photolysis; *ZINC OXIDES --Deposition; *ZINC OXIDES --Photolysis ACOUSTIC ESR; ADHESION;

BREAKDOWN; DEFECTS; DIELECTRIC MATERIALS; DIFFUSION; ELECTRIC CONDUCTIVITY; ELECTRIC POTENTIAL; EXCIMER LASERS; GEOMETRY; GRAIN GROWTH; INFRARED SPECTRA; METALS; MICROELECTRONICS; PARTICULATES; PASSIVATION; PHOTOCHEMISTRY; PYREX; QUARTZ; SPECTROPHOTOMETRY; STRESSES; THIN FILMS IDENTIFIER- ALUMINIUM COMPOUNDS; BOROSILICATE GLASS; CHALCOGENIDES; CHEMICAL REACTIONS; CHEMISTRY; DECOMPOSITION; ELECTRICAL PROPERTIES; ELECTRON SPIN RESONANCE; ELEMENTS; FILMS; GAS LASERS; GLASS; LASERS; MAGNETIC RESONANCE; MATERIALS; MATHEMATICS; MINERALS; NITRIDES; NITROGEN COMPOUNDS; OXIDE MINERALS; OXIDES; OXYGEN COMPOUNDS; PARTICLES; PHOTOCHEMICAL REACTIONS; PHYSICAL PROPERTIES; PNICTIDES; RESONANCE; SILICON COMPOUNDS; SILICON OXIDES; SPECTRA; ZINC COMPOUNDS
SECTIONAL CLASSIFICATION CODE- 360201

Citations from European Fulltext Granted Patents: EFB

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4. Method of producing a CMOS inverter on a soi-substrate with a SIMOX technique

EPB 2000-06-28 0554063/EP-B1 NDN- 080-0136-2848-4

INVENTOR- Inoue, Shunsuke, c/o Canon Kabushiki Kaisha 3-30-2, Shimomaruko, Ohta-ku Tokyo JP
INVENTOR- Koizumi, Toru, c/o Canon Kabushiki Kaisha 3-30-2, Shimomaruko, Ohta-ku Tokyo JP
INVENTOR- Miyawaki, Mamoru, c/o Canon Kabushiki Kaisha 3-30-2, Shimomaruko, Ohta-ku Tokyo JP
INVENTOR- Sugawa, Shigetoshi, c/o Canon Kabushiki Kaisha 3-30-2, Shimomaruko, Ohta-ku Tokyo JP
08902095/WO, A; 04409724/US, A; 63142851/JP
PATENT ASSIGNEE- CANON KABUSHIKI KAISHA 30-2, 3-chome, Shimomaruko, Ohta-ku Tokyo JP DESIGNATED COUNTRIES- DE, FR, GB
PATENT NUMBER- 00554063/EP-B1
PATENT APPLICATION NUMBER- 93300572.0
DATE FILED- 1993-01-27
PUBLICATION DATE- 2000-06-28
PATENT PRIORITY INFORMATION- 4049692, 1992-01-31, JP
FIRM- Beresford, Keith Denis Lewis et al, BERESFORD & Co. High Holborn 2-5 Warwick Court, London WC1R 5DJ, GB
INTERNATIONAL PATENT CLASS- H01L02712
PUBLICATION- 1993-08-04; 2000-06-28, B1, Granted patent
SECONDARY TYPE CITATION-
FILING LANGUAGE- ENG
PROCEDURE LANGUAGE- ENG
DESIGNATED COUNTRY- DE, FR, GB
LANGUAGE- ENG
A semiconductor device has an NMOS transistor and a PMOS transistor formed on at least one monocrystal Si region formed in a thin- film Si layer formed on an insulation layer. The thickness TBOXof the insulation layer on which the NMOS and PMOS transistors are formed, the voltage VSSof a low- voltage power supply and the

voltage VDDof a high- voltage power supply for the NMOS and PMOS transistors satisfy a relationship expressed by the following equation:TBOX> (VDD- V- K(sub)2) /K(sub)1where K(sub)1 (identical with) (epsi)BOX(QBN+ QBP) , K(sub)2 (identical with) 2(phis)FN+ 2(phis)FP- 1.03, (epsi)BOXis the dielectric constant of the base insulation layer, QBNand QBPare bulk charges when the widths of depletion layers of the NMOS and PMOS transistors are maximized, and (phis)FNand (phis)FPare pseudo Fermi potentials of the NMOS and PMOS transistors.
EXEMPLARY CLAIMS- A method of producing a thin-film CMOS inverter circuit comprising:; a monocrystalline silicon bulk semiconductor substrate (1);; an insulation layer (2) on said semiconductor substrate;; a thin-film Si layer (4 to 7,10,11,12,12',13,13') on said insulation layer;; a thin-film NMOS transistor (16) having a source (4,12) and a drain (5,15) in a first isolated monocrystal region (4,5,10,12,12') of said thin-film Si layer, a source electrode (14), a drain electrode (15), and an insulated gate electrode (9);; a thin-film PMOS transistor (17) having a source (7,13') and a drain (6,13) in a second isolated monocrystal region (6,7,11,13,13') of said thin-film Si layer, a source electrode (14'), a drain electrode (15') and an insulated gate electrode (9');; a common input electrode connected to said gate electrode of said NMOS transistor and to said gate electrode of said PMOS transistor;; a common output electrode connected to said drain electrode of said NMOS transistor and to said drain electrode of said PMOS transistor;; a low-voltage power supply, connected to said source electrode of said NMOS transistor, to supply a first voltage, V; volts, thereto; and; a high-voltage power supply connected to said source electrode of said PMOS transistor to supply a second voltage, V; volts, thereto; wherein; the thickness T; BOXof said insulation (2) satisfies a relationship expressed by the following expression:; T; BOX> (V; DD- V; SS- K; 2)/K; 1; where; K; 2(identical with) 2(phis); FN+ 2(phis); - 1.03 Volts,; (epsi); BOXis a dielectric constant of said base insulation layer (2), Q; BNand Q; BPare bulk charges when the widths of depletion layers of said NMOS and PMOS transistors (16,17) are maximized and are expressed in units of Coulombs/cm; 2, and (phis); FNand (phis)
NO-DESCRIPTORS .

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5. Method of enhancing the withstand voltage of a multilayered semiconductor device
EPB 2000-05-31 0419898/EP-B1 NDN- 080-0135-8224-4

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INVENTOR- Mitlehner, Heinz, Dr. Hohenzollernstrasse 104 D-8000 Munchen 40 DE
02738152/DE-A; 04043837/US-A; 04177477/US-A; 04792530/US-A
PATENT ASSIGNEE- SIEMENS AKTIENGESELLSCHAFT Wittelsbacherplatz 2 80333 Munchen DE DESIGNATED COUNTRIES- CH, DE, FR, GB, LI, SE
PATENT NUMBER- 00419898/EP-B1
PATENT APPLICATION NUMBER- 90117012.6
DATE FILED- 1990-09-04
PUBLICATION DATE- 2000-05-31
PATENT PRIORITY INFORMATION- 3932489, 1989-09-28, DE
INTERNATIONAL PATENT CLASS- H01L021332; H01L021331; H01L021263; H01L021225; H01L021266; H01L02932; H01L029167; H01L02974
PUBLICATION- 1991-04-03; 1994-07-20; 2000-05-31, B1, Granted patent
SECONDARY TYPE CITATION-

FILING LANGUAGE- GER
PROCEDURE LANGUAGE- GER
DESIGNATED COUNTRY- CH, DE, FR, GB, LI, SE
LANGUAGE- GER
EXEMPLARY CLAIMS- Method of increasing the dielectric strength of a semiconductor component in wafer form, with four successive layers: an emitter layer (1) of a first conductivity type, a base layer (2) of a second conductivity type, a base layer (3) of the first conductivity type and a second emitter layer (4) of the second conductivity type, in which the emitter layer of the first conductivity type has a connection to a cathode (K) and the emitter layer of the second conductivity type has a connection to the anode (A), and in which there is a first pn junction (7) between the base layer of the first conductivity type and the base layer of the second conductivity type and a second pn junction (8) between the base layer of the first conductivity type and the emitter layer of the second conductivity type, characterized in that a central active region (LBz) of the semiconductor component is covered with an exposure mask in such a way that proton exposure of the semiconductor component takes place only in a region (LBr) of positively bevelled edge connections (12, 13) which are provided in order to reduce the surface field strength, in that a relatively thin zone (16, 17) in comparison with the thickness of the base layer of the first conductivity type is created in the lateral region (LBr) outside the exposure mask and vertically between the first and second pn junctions, the thin zone (16) having a reduced charge-carrier lifetime compared with the base layer of the first conductivity type and the exposure energy of the proton radiation being designed such that the thin zone with the reduced charge-carrier lifetime lies outside the space-charge zone created as a result of the reverse blocking voltage at the first and/or second pn junction (7, 8).
NO-DESCRIPTORS .

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6. PROCESS FOR MANIPULATING MICROSCOPICALLY SMALL DIELECTRIC PARTICLES AND DEVICE FOR IMPLEMENTING THE PROCESS
EPB 1996-02-07 0555252/EP-B1 NDN- 080-0089-3105-9

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INVENTOR- WAGNER, Bernd Potsdamer Ch. 31c D-1000 Berlin 38 DE
INVENTOR- FUHR, Gunter Str. 64, Nr. 6, 13-19 D-1113 Berlin DE
INVENTOR- HAGEDORN, Rolf Wartinerstr. 16 D-1094 Berlin DE
INVENTOR- MULLER, Thorsten Hartriegelstr. 100 D-1190 Berlin DE
PATENT ASSIGNEE- FRAUNHOFER-GESELLSCHAFT ZUR FORDERUNG DER ANGEWANDTEN FORSCHUNG E. V. Leonrodstrasse 54 80636 Munchen DE
DESIGNATED COUNTRIES- CH, DE, FR, GB, IT, LI, NL
PATENT NUMBER- 00555252/EP-B1
PATENT APPLICATION NUMBER- 91918107.3
DATE FILED- 1991-10-28; 1991-10-28
PUBLICATION DATE- 1996-02-07
PATENT PRIORITY INFORMATION- 4034697, 1990-10-31, DE
FIRM- Munich, Wilhelm, Dr. et al, Kanzlei Munich, Steinmann, Schiller Wilhelm-Mayr-Str. 11, 80689 Munchen, DE
INTERNATIONAL PATENT CLASS- B03C00500; B03C00502; G01N01500
PCT PUBLICATION DATE- 1992-05-14
PUBLICATION- 1993-08-18; 1993-08-18; 1996-02-07, B1, Granted patent
SECONDARY TYPE CITATION-
FILING LANGUAGE- GER

PROCEDURE LANGUAGE- GER
DESIGNATED COUNTRY- CH, DE, FR, GB, IT, LI, NL
LANGUAGE- GER
EXEMPLARY CLAIMS- Device for manipulating microscopic dielectric particles, comprising:; a substrate body,; a multi- electrode system disposed on said substrate body for generating a travelling electric field, and including electrodes disposed adjacent to each other approximately orthogonally to the travelling direction of said travelling field, and; an electronic circuit for successive application of appropriate electrical voltages to said electrodes,; in that both the spacing and the widths of said electrodes are smaller than the diameter of the particles to the manipulated, and that the travelling frequencies of said electric fields range from 0.1 to 100 MHz.; Device according to Claim 1,; in that said electrodes present an elongate rectangular shape and are equidistantly disposed in parallel to each other such that the direction of said travelling field extends orthogonally to the longitudinal axes of said electrodes.; Device according to Claim 1 or 2,; in that, starting out from an electrode in the central region of said multi-electrode system, said electrodes present discontinuities in a region diverging in V-shape in the direction of said travelling field, wherein said electrodes are bent off in the vicinity of said discontinuity in such a way that they open at right angles into said V- shaped region.; Device according to any of Claims 1 to 3,
NO-DESCRIPTORS .

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7. SEMICONDUCTOR FILM BOLOMETER THERMAL INFRARED DETECTOR
EPB 1996-12-11 0526551/EP-B1 NDN- 080-0087-3408-1

INVENTOR- LIDDIARD, Kevin, Charles 18 Ferrier Avenue Fairview Park, S.A. 5126 AU
PATENT ASSIGNEE- THE COMMONWEALTH OF AUSTRALIA c/o the Secretary Department of Defence Support, Anzac Park West Building, Constitution Avenue Canberra, Australian Capital Territory 2600 AU DESIGNATED COUNTRIES- BE, CH, DE, FR, GB, IT, LI, NL, SE
PATENT NUMBER- 00526551/EP-B1
PATENT APPLICATION NUMBER- 91908757.7
DATE FILED- 1991-04-24; 1991-04-24
PUBLICATION DATE- 1996-12-11
PATENT PRIORITY INFORMATION- 981390, 1990-04-26, AU
FIRM- Opperman, Stuart Richard et al, Haseltine Lake & Co. Hazlitt House 28 Southampton Buildings Chancery Lane, London WC2A 1AT, GB
INTERNATIONAL PATENT CLASS- G01J00520
PCT PUBLICATION DATE- 1991-10-31
PUBLICATION- 1993-02-10; 1996-12-11, B1, Granted patent
SECONDARY TYPE CITATION-
FILING LANGUAGE- ENG
PROCEDURE LANGUAGE- ENG
DESIGNATED COUNTRY- BE, CH, DE, FR, GB, IT, LI, NL, SE
LANGUAGE- ENG
EXEMPLARY CLAIMS- An infrared detector comprising a supporting substrate (6) with a cavity formed therein, a dielectric pellicle (5) of low thermal conductivity material suspended over the cavity in the substrate (6) and a heat-sensitive layer (1) with thin metallic contacts (9) thereto deposited on the pellicle (5), characterised in that the dielectric pellicle (5) includes holes or slots (8) through which the cavity is

formed by etching and the heat-sensitive layer (1) with thin metallic contacts (9) is an optical interference filter in which a heat-sensitive semiconductor layer (3) is sandwiched between first and second thin film metallic contacts formed as layers (2, 4), the thickness of the heat- sensitive semiconductor layer (3) being substantially equal to one quarter of the wavelength ((lambda)) of the infrared wavelength to be detected, multiplied by its refractive index (n).; An infrared detector according to claim 1, characterised in that the supporting substrate (6) is a monocrystaline silicon wafer and the cavity is formed by anisotropic etching using a chemical etchant selected from hydrazine, ethylene diamine pyrocatechol or potassium hydroxide.; An infrared detector according to claim 1 or 2, characterised in that the first conductor layer (2) has a resistance of less than 10 ohms per square and the second conductor layer (4) has a resistance of between 300 and 500 ohms per square, the second layer (4) being disposed above the first layer (2) in order to receive the first infrared radiation to be detected.; An infrared detector according to claim 1, 2 or 3, characterised in that the heat-sensitive semiconductor layer (3) is a layer of silicon prepared by sputter or chemical vapour deposition.; An infrared detector according to any one of the preceding claims, characterised in that the thin film metallic layers (2, 4) are formed from one or more layers of nickel, nickel-chromium, platinum, platinum silicide or tantalum silicide.
NO-DESCRIPTORS .

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8. Process for cleaning oxidized metallic surfaces in the fabrication of interconnection networks and boards for such networks
EPB 1996-03-06 0518774/EP-B1 NDN- 080-0086-8425-2

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00129490/EP-A; 00300414/EP-A; 00387097/EP-A; 04706870/US-A
PATENT ASSIGNEE- FRANCE TELECOM 6, Place d'Alleray 75015 Paris FR
DESIGNATED COUNTRIES- DE, GB
PATENT NUMBER- 00518774/EP-B1
PATENT APPLICATION NUMBER- 92401628.0
DATE FILED- 1992-06-12
PUBLICATION DATE- 1996-03-06
PATENT PRIORITY INFORMATION- 9107325, 1991-06-14, FR
FIRM- Casalonga, Axel et al, BUREAU D.A. CASALONGA - JOSSE Morassistrasse 8, 80469 Munchen, DE
INTERNATIONAL PATENT CLASS- C23G00500; C23C01650; H01L021768; H01L021321
PUBLICATION- 1992-12-16; 1992-12-16; 1996-03-06, B1, Granted patent
SECONDARY TYPE CITATION-
FILING LANGUAGE- FRE
PROCEDURE LANGUAGE- FRE
DESIGNATED COUNTRY- DE, GB
LANGUAGE- FRE
une premiere couche conductrice metallisee,une couche dielectrique deposee sur la couche metallisee, puis gravee pour denuder les surfaces a metalliser ou trous de contact, etune seconde couche metallisee deposee sur la surface gravee, caracterise en ce que les plaquettes gravees sont traitees par plasma multipolaire micro-onde

sous hydrogene avant le depot de la seconde couche metallisee.Elle concerne egalement les plaquettes pour reseaux d'interconnexions dans lesquels les surfaces metallisees ont ete nettoyees selon l'invention.
EXEMPLARY CLAIMS- A process for cleaning oxidized metallized surfaces, employed in the manufacture of wafers for interconnection networks, comprising at least:; a first metallized conducting layer,; a dielectric layer deposited on the metallized layer and then etched in order to bare the surfaces to be metallized or contact holes, and; a second metallized layer deposited on the etched surface, wherein the etched wafers are treated using microwave multipolar plasma under hydrogen before the deposition of the second metallized layer.; The process as claimed in claim 1, wherein the first metallized conducting layer and/or the second metallized conducting layer essentially consists or consist of copper, nickel or tungsten.; The process as claimed in claim 1 or 2, wherein the first metallized conducting layer and/or the second metallized conducting layer essentially consists or consist of copper.; The process as claimed in one of claims 1 to 3, wherein the treatment using microwave multipolar plasma is carried out at a temperature lying between 0.C and 400.C.; The process as claimed in one of claims 1 to 4, wherein the treatment using microwave multipolar plasma under hydrogen is carried out at ambient temperature.; The process as claimed in one of claims 1 to 5, wherein the treatment using microwave multipolar plasma is assisted by bias of the substrate, the bias voltage varying from 0 to 1000 volts.; The process as claimed in one of claims 1 to 6, wherein the treatment using microwave multipolar plasma under hydrogen is carried out in the same chamber as the deposition.; The process as claimed in one of claims 1 to 7, wherein the treatment using microwave multipolar plasma under hydrogen is directly preceded by an etching treatment using microwave multipolar plasma under oxygen.; Procede de nettoyage de surfaces metallisees oxydees mises en oeuvre dans la fabrication des plaquettes pour reseaux d'interconnexions, comportant au moins :; une premiere couche conductrice metallisee,
NO-DESCRIPTORS .

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9. Heat treatment of Si single crystal
EPB 1996-09-18 0503816/EP-B1 NDN- 080-0085-8741-4

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INVENTOR- Yamagishi, Hirotoshi Annaka 1721-3, Annaka-shi Gunma- ken JP
INVENTOR- Fujimaki, Nobuyoshi Yanase 117-201, Annaka-shi Gunma- ken JP

INVENTOR- Karasawa, Yukio Koh 856, Kenzaki-machi Takasaki-shi, Gunma- ken JP
00390672/EP-A; 02080780/GB-A; 02182262/GB-A; 57200293/JP-A
PATENT ASSIGNEE- SHIN-ETSU HANDOTAI COMPANY LIMITED 4-2, Marunouchi 1-Chome Chiyoda-ku Tokyo JP DESIGNATED COUNTRIES- DE, FR, GB
PATENT NUMBER- 00503816/EP-B1
PATENT APPLICATION NUMBER- 92301795.8
DATE FILED- 1992-03-03
PUBLICATION DATE- 1996-09-18
PATENT PRIORITY INFORMATION- 76876/91, 1991-03-15, JP
FIRM- Pacitti, Pierpaolo A.M.E. et al, Murgitroyd and Company 373 Scotland Street, Glasgow G5 8QA, GB
INTERNATIONAL PATENT CLASS- C30B03302; C30B01500; C30B02906
PUBLICATION- 1992-09-16; 1992-09-16; 1996-09-18, B1, Granted patent

SECONDARY TYPE CITATION-
FILING LANGUAGE- ENG
PROCEDURE LANGUAGE- ENG
DESIGNATED COUNTRY- DE, FR, GB
LANGUAGE- ENG
The method of this Invention for heat treatment of a Si single crystal grown by the Czochralski method at a speed of pull of not less than 0.8 mm/min., characterized by heat-treating at a temperature in the range of from 1,150 .C to 1,280 .C a wafer cut out of the SI single crystal thereby producing a Si wafer excellent in oxide film dielectric breakdown voltage characteristic due to elimination of crystal defects. Consequently, this invention ensures production of LSI in a high yield.
EXEMPLARY CLAIMS- A method for heat treatment of a wafer cut out of a Si single crystal bar grown by the Czochralski method at a speed of pull exceeding 0.8 mm/min. and not higher than 1.6 mm/min. at a temperature in the range 1150.C to 1280.C for the purpose of obtaining a Si single crystal wafer with an improved oxide film dielectric breakdown voltage; characterised by:; determining, in advance, a first correlation between the oxide film breakdown voltage and the density of scale-like patterns as obtained by selective etching of the wafer, and a second correlation between said density of scale-like patterns and the time period of the heat treatment; and; heat treating the Si single crystal wafer within said temperature range in an atmosphere of dry oxygen for a time period of at least 10 minutes, selected on the basis of said first and second correlations such that the Si single crystal wafer has a density of scale-like patterns not higher than 200 counts/cm; after the heat treatment, which is required to improve the oxide film dielectric breakdown voltage to not less than 8MV/cm.; The method for heat treatment as claimed in Claim 1, wherein the time period of the heat treatment is selected on the basis of said correlation such that a wafer having a density of scale-like patterns between 500 counts/cm; 2and 3000 counts/cm; 2in advance of the heat treatment has said density of scale-like patterns no higher than 200 counts/cm; after the heat treatment.; Methode de traitement thermique d'une galette decoupee dans un barreau de Si monocristallin obtenu par tirage selon le procede Czochralski a une vitesse de tirage superieure a 0,8 mm/min mais ne depassant pas 1,6 mm/min, a une temperature comprise entre 1150 et 1280.C, afin d'obtenir une galette de Si monocristallin ayant une meilleure tension dielectrique de claquage du film d'oxyde,; caracteriseeen ce qu'elle comprend :
NO-DESCRIPTORS .

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10. Method for testing electrical properties of silicon single crystal
EPB 1996-06-05 0487302/EP-B1 NDN- 080-0084-8883-7

INVENTOR- Fusegawa, Izumi Yanase 791-4 Annaka-shi, Gunma-ken JP
INVENTOR- Yamagishi, Hirotoshi Annaka 1721-3 Annaka-shi, Gunma- ken JP
INVENTOR- Fujimaki, Nobuyoshi Yanase 117-201 Annaka-shi, Gunman- ken JP
INVENTOR- Karasawa, Yukio Koh 856, Kenzaki-machi Takasaki-shi, Gunma- ken JP
03223664/DE, A; 60146000/JP; 52122479/JP; 63215041/JP; 000220707/XP
PATENT ASSIGNEE- SHIN-ETSU HANDOTAI COMPANY LIMITED 4-2, Marunouchi 1-Chome Chiyoda-ku Tokyo JP DESIGNATED COUNTRIES- DE, FR, GB
PATENT NUMBER- 00487302/EP-B1
PATENT APPLICATION NUMBER- 91310648.0

DATE FILED- 1991-11-19
PUBLICATION DATE- 1996-06-05
PATENT PRIORITY INFORMATION- 320467/90, 1990-11-22, JP
FIRM- Pacitti, Pierpaolo A.M.E. et al, Murgitroyd and Company 373 Scotland Street, Glasgow G5 8QA, GB
INTERNATIONAL PATENT CLASS- G01N02792; C30B03300; C30B03308
PUBLICATION- 1992-05-27; 1993-11-18; 1996-06-05, B1, Granted patent
SECONDARY TYPE CITATION-
FILING LANGUAGE- ENG
PROCEDURE LANGUAGE- ENG
DESIGNATED COUNTRY- DE, FR, GB
LANGUAGE- ENG
The evaluation of the oxide film dielectric breakdown voltage of a silicon semiconductor single crystal is caried out by cutting a wafer out of the single crystal rod, etching the surface of the wafer with the mixed solution of hydrofluoric acid and nitric acid thereby relieving the wafer of strain, then etching the surface of the wafer with the mixed solution of K(sub)2Cr(sub)2O(sub)7, hydrofluoric acid, and water therby inducing occurrence of pits and scale-like patterns on the surface, determining the density of the scale-like patterns, and computing the oxide film dielectric breakdown voltage by making use of the correlating between the density of scale-like patterns and the oxide film dielectric breakdown voltage. This fact established the method of this invention to be capable of effecting an evaluation equivalent to the evaluation of the oxide film dielectric breakdown voltage of a PW wafer prepared from the single crystal rod.
EXEMPLARY CLAIMS- A method for testing electrical properties of a silicon single crystal, characterized by pulling up a silicon semiconductor single crystal by the Czochralski method or the floating zone pulling method, cutting a wafer of a prescribed thickness from said single crystal, etching the surface of the wafer with a mixed solution of hydrofluoric acid and nitric acid thereby relieving said wafer of strain, then setting the wafer upright in a mixed solution of K; 2Cr; 2O; , hydrofluoric acid and water and selectively etching the surface of the wafer therein for a period in the range from 10 to 60 minutes, and taking count of the number of scale-like patterns consequently appearing on the surface of the wafer, thereby evaluating the oxide film dielectric breakdown voltage of said silicon single crystal.; Methode pour controler les proprietes electriques d'un monocristal de silicium, caracterisee en que :; on realise un monocristal de silicium semiconducteur par la methode de Czochralski ou la methode de la zone flottante,; on decoupe une galette d'epaisseur determinee dudit monocristal,; on grave la surface de la galette par application d'une solution d'acide fluorhydrique et d'acide nitrique pour degager ladite galette des contraintes,; ensuite, on place verticalement la galette dans une solution de K; 2Cr; 2O; , d'acide fluorhydrique et d'eau,; puis on grave selectivement la surface de la galette au sein de cette solution pendant des periodes de duree comprises entre 10 et 60 minutes,; enfin, on compte le nombre de motifs en forme de depot apparaissant a la surface de la galette pour ainsi evaluer la tension dielectrique de claquage du film d'oxyde dudit monocristal de silicium.
NO-DESCRIPTORS .

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11. Low temperature plasma nitridation process and applications of nitride films formed thereby
EPB 1995-08-09 0201380/EP-B1 NDN- 080-0064-9017-3

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INVENTOR- Petro, William G. 10369 Leola Court Cupertino California 95014 US
INVENTOR- Barry, Michael L. 1221 Dana Avenue Palo Alto California 94301 US

00015694/EP-A
PATENT ASSIGNEE- FAIRCHILD SEMICONDUCTOR CORPORATION 10400 Ridgeview Court P.O. Box 1500 Cupertino, California 95014 US DESIGNATED COUNTRIES- DE, FR, GB, IT, NL
PATENT NUMBER- 00201380/EP-B1
PATENT APPLICATION NUMBER- 86400742.2
DATE FILED- 1986-04-08
PUBLICATION DATE- 1995-08-09
PATENT PRIORITY INFORMATION- 721422, 1985-04-09, US; 801955, 1985-11-26, US
FIRM- Sparing Rohl Henseler Patentanwalte, Postfach 14 04 43, 40074 Dusseldorf, DE
INTERNATIONAL PATENT CLASS- H01L021318; H01L02943
PUBLICATION- 1986-12-17; 1988-01-13; 1995-08-09, B1, Granted patent
SECONDARY TYPE CITATION-
FILING LANGUAGE- ENG
PROCEDURE LANGUAGE- ENG
DESIGNATED COUNTRY- DE, FR, GB, IT, NL
LANGUAGE- ENG

A silicon nitride layer is prepared on the surface of a silicon substrate by carrying out a surface reaction on the substrate in a vacuum chamber that contains an electrode which is capacitively coupled to an rf generator. A second electrode within the chamber, or a metal wall of the chamber itself, is connected to ground. The silicon substrates to be treated are placed on one of the electrodes to be in electrical and physical contact therewith, and a reagent gas that contains nitrogen is introduced into the chamber. An rf voltage is then applied between the electrodes to ionize and activate the gas, and cause ions and other active species thereof to be directed into the silicon substrate. The nitrogen ions and other active species that are created as a result of the application of the rf power can be directed at the surface of a number of wafers simultane-ously. The thin nitride films that are formed by the process have application both as barriers for device isolation and as dielectric components of electrical devices.

EXEMPLARY CLAIMS- A method of preparing a thin film of silicon nitride or other nitrogen-containing composition on a silicon substrate,; comprising the steps of: placing one surface of silicon substrate in contact with a first of a pair of plate electrodes, said first electrode being spaced away and opposite from a second plate electrode of said pair of electrodes which faces the opposite surface of said substrate and has an area greater than said first of said pair of electrodes; evacuating a chamber in which said electrodes and the substrate are located; introducing a nitrogen-containing reagent gas free of silicon compounds into the space between said pair of electrodes; and applying an a.c. voltage having a frequency of about 10 KHz or greater between said electrodes to thereby ionize and activate the reagent gas and accelerate ions thereof into the substrate while cooling said first of said pair of electrodes to inhibit heating of said substrate wherein the temperature of said substrate is less than 200.C.; The method of claim 1 wherein said reagent gas

comprises one of pure nitrogen, ammonia and a nitrogen-hydrogen mixture.; The method of claim 1 further including the step of annealing the thin film of nitride formed on said substrate.; The method of claim 3 wherein said annealing step is carried out in the presence of a non- oxidizing gas.; The method of claim 1 wherein the area of the other electrode of said pair of electrodes is at least twice as great as the area of said one electrode.; The method of one of the preceding claims for isolating active regions from one another in an integrated circuit , comprising the steps of: removing selected portions of said film so that the remaining portions of the film correspond to areas in which active devices are to be formed in the wafer; and oxidizing the areas on said surface of the wafer that are not covered by the remaining portions of the nitride film.
NO-DESCRIPTORS .

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12. In situ monitoring technique and apparatus for chemical/mechanical planarization endpoint detection
EPB 1994-09-07 0455455/EP-B1 NDN- 080-0061-2955-7

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02895264/US-A; 03063206/US-A; 59129664/JP-A
PATENT ASSIGNEE- AT&T Corp. 32 Avenue of the Americas New York, NY 10013-2412 US DESIGNATED COUNTRIES- DE, DK, ES, FR, GB, IT, NL, SE
PATENT NUMBER- 00455455/EP-B1
PATENT APPLICATION NUMBER- 91303869.1
DATE FILED- 1991-04-29
PUBLICATION DATE- 1994-09-07
PATENT PRIORITY INFORMATION- 517106, 1990-05-01, US
FIRM- Johnston, Kenneth Graham et al, Lucent Technologies (UK) Ltd, 5 Mornington Road, Woodford Green Essex, IG8 OTU, GB
INTERNATIONAL PATENT CLASS- B24B03704; B23Q015007
PUBLICATION- 1991-11-06; 1992-04-15; 1994-09-07, B1, Granted patent
SECONDARY TYPE CITATION-
FILING LANGUAGE- ENG
PROCEDURE LANGUAGE- ENG
DESIGNATED COUNTRY- DE, DK, ES, FR, GB, IT, NL, SE
LANGUAGE- ENG
This invention provides an in situ monitoring technique and apparatus (20) for chemical/mechanical planarization end point detectionin the process of fabricating semiconductor or optical devices. Fabrication of semiconductor or optical devices often requires smooth planar surfaces, either on the surface of a wafer (2) being processed or at some intermediate stage e.g. a surface of an interleaved layer. The detection in the present invention is accomplished by means of capacitively measuring the thickness of a dielectric layer (4) on a conductive substrate. The measurement involves the dielectric layer (4), a flat electrode structure (25) and a liquid (20) interfacing the article and the electrode structure. Polishing slurry acts as the interfacing liquid. The electrode structure includes a measuring electrode (26), an insulator surrounding the measuring electrode (28,29), a guard electrode (27) and another insulator surrounding the guard electrode. In the measurement a drive voltage is supplied to the measuring electrode, and in a bootstrap arrangement to a

surrounding guard electrode, thereby measuring the capacitance of the dielectric layer of interest without interfering effect from shunt leakage resistance. The process and apparatus are useful not only for measuring the thickness of dielectric layers on conductive substrates in situ, during planarizing polishing, but also for measuring the dielectric thickness on substrates in other processes, e.g. measuring the dielectric layer thickness prior to or after an etching process.
EXEMPLARY CLAIMS- A process for in situ monitoring the thickness of a dielectric material (4) on a surface (5) of an electrically conductive substrate (2) having less than about one megohm-cm resistivity, characterised by placing the substrate so that a surface of an electrode structure (25) faces the dielectric material, interposing between the substrate and the surface of the electrode structure a film of a conductive liquid (20) with resistivity of less than about 100,000 ohm-cm, said film being in contact with the dielectric material (4) and the surface of the electrode structure, and measuring the capacitance between the substrate (2) and the electrode structure (25).; The process of claim 1 or 14, wherein said measuring includes measuring the capacitance and simultaneously removing from the result the effects of leakage resistance paths.; The process of claim 1, 2, or 14, wherein the capacitive measurement comprises applying a measuring voltage to a measuring electrode (26) of the electrode structure (25) and a bootstrapping guard voltage to a narrow conductive area surrounding the measuring electrode, said measuring electrode and said narrow conductive area being insulated each from another with or without another insulator surrounding the guard electrode (27).; The process of claim 3 or 14, wherein said measuring comprises maintaining constant displacement current resulting from said voltage application, the amplitude of the drive voltage thereby being proportional to the thickness of the dielectric layer (4).
NO-DESCRIPTORS .

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13. A programmable element for a semiconductor integrated circuit chip
EPB 1991-01-23 0224418/EP-B1 NDN- 080-0020-9005-0

INVENTOR- Nawata, Takahiro 3, Azamino 4-chome Midori-ku Yokohama- shi Kanagawa 227 JP
INVENTOR- Wada, Kunihiko Pakusaido Musashikosugi 403 658-1, Miyauchi Nakahara-ku Kawasaki-shi Kanagawa 211 JP
INVENTOR- Sato, Noriaki 28-21, Tsurukawa 4-chome Machida-shi Tokyo 194-01 JP
03576549/US-A; 03793090/US-A; 0000####; 57103348/JP-A
PATENT ASSIGNEE- FUJITSU LIMITED 1015, Kamikodanaka, Nakahara-ku Kawasaki-shi, Kanagawa 211 JP DESIGNATED COUNTRIES- DE, FR, GB
PATENT NUMBER- 00224418/EP-B1
PATENT APPLICATION NUMBER- 86402644.8
DATE FILED- 1986-11-28
PUBLICATION DATE- 1991-01-23
PATENT PRIORITY INFORMATION- 268539/85, 1985-11-29, JP
FIRM- Descourtieux, Philippe et al, Cabinet Beau de Lomenie 158, rue de l'Universite, 75340 Paris Cedex 07, FR
INTERNATIONAL PATENT CLASS- H01L02710; G11C01700
PUBLICATION- 1987-06-03; 1987-06-03; 1991-01-23, B1, Granted patent
SECONDARY TYPE CITATION-
FILING LANGUAGE- ENG
PROCEDURE LANGUAGE- ENG

DESIGNATED COUNTRY- DE, FR, GB
LANGUAGE- ENG
A programmable element for a semiconductor integrated cir- cuit device is formed from a couple of electrode layers(34,36) and an insulating layer (31) intervening therebetween and is programmed by applying a voltage between the electrode layers to cause an electrical breakdown and form a conduction path in the insulating layer. The insulting layer (31) comprises two films (32,33) of different dielectric materials, such as silicon nitride and silicon-dioxide successively formed on the lower electrode layer. Typically, the Si(sub)3N(sub)4 film has a thickness in the range between 5 and 20 nm and the SiO(sub)2 film has a thickness in the range between 05 and 10 nm. The composite structure of the insulating layer results in a relatively low programming voltage and a reduced resistance of a programmed BIC cell.
EXEMPLARY CLAIMS- 1. A programmable element for a semiconductor integrated circuit chip, comprising a lower electrode layer (34) formed on a substrate (35); a first insulating layer (31) formed on the lower electrode layer; and an upper electrode layer (36) formed on the first insulating layer, the upper electrode being separated from the lower electrode by the first insulating layer, whereby the programmable element is provided with a conduction path between the lower and upper electrodes when a voltage capable of causing an electrical breakdown in the first insulating layer is applied between the lower and upper electrodes, characterized in that said first insulating layer (31) is composed of at least two films (32, 33) of dielectric materials, successively formed on said lower electrode layer (34), said dielectric material films having respective specific dielectric constants different from each other.; 2. A programmable element according to claim 1, wherein one of said dielectric films is a silicon-nitride film (32).; 3. A programmable element according to any one of claims 1 and 2, wherein one of said dielectric films is a silicon-dioxide film (33).; 4. A programmable element according to any one of claims 1 to 3, wherein said first insulating layer comprises a relatively thin silicon-dioxide film (33) and a relatively thick silicon-nitride film (32).; 5. A programmable element according to any one of the preceding claims, wherein one of said dielectric films is a silicon-nitride film (32) having a thickness in a range from 5 nm to 20 nm.; 6. A programmable element according to any one of the preceding claims, wherein one of said dielectric films is a silicon-dioxide film (33) having a thickness in a range from 0.5 nm to 10 nm.
NO-DESCRIPTORS .

Citations from Engineering Index: EI1

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14. Surface micromachined pressure transducers.
EIX 92-01 EIX92010003824 NDN- 017-0162-4540-3

AUTHORS- Guckel, H.
Sens Actuators A Phys v 28 n 2 Jul 1991 p 133-146
PUBLICATION DATE- 1991
DOCUMENT TYPE- JA, Journal Article
ISSN- 0924-4247
CODEN- SAAPEB
AUTHOR AFFILIATION- Univ of Wisconsin, Madison, WI, USA
MONTHLY PUBLICATION NUMBER- 010241

JOURNAL NAME- Sensors and Actuators, A: Physical
LANGUAGE- English
Typical IC processing is fundamentally two dimensional; sensors are three-dimensional structures. In surface micromachining, two-dimensional IC processing is extended to sensor structures by the addition of one or more sacrificial layers which are removed by lateral etching. The resulting sensor structures involve the substrate and one or more deposited films which form the intended micromechanical component. The concepts of this type of sensor manufacturing are readily demonstrated by considering absolute pressure transducers in some detail. Absolute pressure transducers involve a vacuum-sealed cavity and a deformation sensing technique. The cavity is formed from the substrate and a low-pressure chemical vapor deposited polycrystalline silicon film. The mechanical properties of this film must be controlled well enough to allow the device to be designed. This implies morphological control during processing. Optimized films which do exhibit controlled compressive or tensile strains exclude oxygen or nitrogen and are therefore not modified by extended hydrofluoric acid etches. Their mechanical behavior is monitored by micromechanical test structures which measure Euler buckling and thereby determine the value of the built-in strain. The cavity vacuum is established by reactive sealing. Long-term vacuum integrity is achieved by a low-stress silicon nitride barrier which also acts as a dielectric isolation barrier. Sensing is accomplished via deposited polysilicon resistors. These devices behave like metal resistors in terms of their temperature coefficient of resistance and noise figure. Their piezoresistive behavior is larger than that of typical metal film structures and smaller than that of single-crystal resistors. Pressure sensors with four diaphragms, two active and two inactive, have been constructed and optimized towards manufacturability. The measured performance is excellent and agrees with the predictions of the design algorithm. (Author abstract) 40 Refs.
DESCRIPTOR- INTEGRATED CIRCUITS ; PIEZOELECTRIC TRANSDUCERS; SEMICONDUCTING SILICON --Films; SENSORS
IDENTIFIER- MICROMACHINING; POLYSILICON
TREATMENT CODE- TC-X (Experimental); TC-T (Theoretical)
SECTIONAL CLASSIFICATION CODE- CAL944; CAL714; CAL712; CAL531; CAL933; CAL704
SECTION HEADING- PRESSURE TRANSDUCERS --Performance

Citations from Engineering Index: EI2

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15. Measurement of polyimide interlayer adhesion using microfabricated structures.

EIX 89-05 EIX89050045495 NDN- 163-0241-9685-5

AUTHORS- Allen, Mark G.; Senturia, Stephen D.
Polymeric Materials Science and Engineering, Proceedings of the ACS Division of Polymeric Materials Science and Engineering v 59. Publ by ACS, Books & Journals Division, Washington, DC, USA. p 352-356
PUBLICATION DATE- 1988
DOCUMENT TYPE- CA, Conference Paper
ISSN- 0743-0515
CODEN- PMSEDG

AUTHOR AFFILIATION- MIT, Cambridge, MA, USA
PATENT REFERENCE- Polymeric Materials Science and Engineering, Proceedings of the ACS Division of Polymeric Materials Science and Engineering
PATENT STATUS INFORMATION- 045536
CONFERENCE DATE- 19880926-19880930
CONFERENCE TITLE- Proceedings of the ACS Division of Polymeric Materials: Science and Engineering - Fall Meeting
CONFERENCE LOCATION- Los Angeles, CA, USA
LANGUAGE- English
The adhesion of polymer layers is extremely important in many integrated circuit multilevel metal interconnect schemes. Cracks between layers can result in moisture ingression and corrosion of metal lines, leading to long term device reliability problems. In addition, catastrophic delamination, (for example, induced by film stress) can result in the sudden and immediate failure of the device. In spite of the importance of interlayer adhesion, few tests are available which can measure quantitatively and in-situ the energy necessary to debond these films. Preliminary work has focused primarily on the peel test. However, the peel test suffers from two shortcomings which limit its utility. First, loading the sample is difficult; grasping one layer of film while keeping the others adhered can be a problem. Second, and most importantly, the peel test can be tensile strength limited. If the layers to be peeled apart are very thin and also well-adhered, tearing instead of interlayer debonding may occur. In this case, it is not possible to make a measurement of the debond energy of the film. The authors developed a modification of the standard blister test, called the 'island blister', which can overcome this tensile strength limit, as well as allow a convenient method of loading the film. The test and its application to the problem of polyimide interlayer adhesion are discussed in this paper. 12 Refs.
DESCRIPTOR- ADHESION --Testing; FILMS --Dielectric; INTEGRATED CIRCUITS --Reliability
IDENTIFIER- BLISTER TEST; CATASTROPHIC DELAMINATION; FILM STRESS EFFECTS; INTEGRATED CIRCUIT MULTILEVEL METAL INTERCONNECT SCHEMES; MICROFABRICATED STRUCTURES; POLYIMIDE INTERLAYER ADHESION
TREATMENT CODE- TC-G (General Review); TC-X (Experimental)
SECTIONAL CLASSIFICATION CODE- CAL815; CAL817; CAL801; CAL931; CAL713; CAL714
SECTION HEADING- POLYIMIDES --Adhesion

Citations from INSPEC: IN2

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16. Residual stress in PZT thin films and its effect on ferroelectric properties
INS 93-51 4565984 A9403-6860-003 (PHA) NDN- 083-0456-5984-0

AUTHORS- Garino, T. J.; Harrington, H. M.
EDITOR- Kingon, A. I.; Myers, E. R.; Tuttle, B.
ABBREVIATED JOURNAL TITLE- Ferroelectric Thin Films II Symposium
PUBLICATION DATE- 1992
PP 341-7
xvii+585 PAGES
16 REFERENCES
DOCUMENT TYPE- Conference paper

CORPORATE AUTHOR- Sandia Nat. Labs., Albuquerque, NM, USA
PUBLISHER- Mater. Res. Soc
PUBLICATION PLACE- Pittsburgh, PA, USA
PUBLICATION COUNTRY- USA
CONFERENCE DATE- 2-4 Dec. 1991
CONFERENCE LOCATION- Boston, MA, USA
LANGUAGE- English (DEF)
The residual stress in solution derived Pb(Zr/sub 0.53/Ti/sub 0.47/)O/sub 3/, PZT 53:47, films was determined by measuring the bending of the substrate due to the stress. The substrate consisted of an oxidized (100) silicon wafer with 300 nm coating of platinum. In all cases the stress was tensile. Films fired at a temperature in the range where pyrochlore formation occurs (500 degrees to 575 degrees C) had the highest residual stresses, 200 to 350 MPa, whereas those fired at higher temperatures, 600 degrees to 650 degrees C, where the perovskite phase forms had stresses of 100 to 200 MPa. Stress measurements made during film firing indicate that the pyrochlore containing films had higher residual stress because their coefficient of thermal expansion was much larger than that of predominantly perovskite films. The effect of the amount of stress on ferroelectric properties was studied by making measurements on a film with and without the application of an external stress. The external stress was applied by bending a circular section of the substrate, which effectively lowered the amount of tensile stress in the film by -30%. Decreasing the stress in this manner was found to increase the remanent polarization by -11% and the dielectric constant by -2%.
DESCRIPTOR- dielectric polarisation; ferroelectric materials; ferroelectric thin films; internal stresses; lead compounds; permittivity; thermal expansion
IDENTIFIER- bending; dielectric constant; external stress; ferroelectric properties; film firing; perovskite phase; pyrochlore formation; remanent polarization; residual stress; substrate; tensile stress; thermal expansion; Pb(Zr/sub 0.53/Ti/sub 0.47/)O/sub 3/; PbZrO3TiO3; Pt; PZT; PZT thin films; SiO/sub 2/; 500 to 650 degC

NUMERICAL DATA INDEXING- temperature 7.73E+02 to 9.23E+02 K
CHEMICAL INDEXING- PbZrO3TiO3/ss TiO3/ss ZrO3/ss O3/ss Pb/ss Ti/ss Zr/ss O/ss; Pt/sur Pt/el; SiO2/sur O2/sur Si/sur O/sur SiO2/bin O2/bin Si/bin O/bin
TREATMENT CODE- TC-X
SECTIONAL CLASSIFICATION CODE- A6860; A7780; A7755; A7730; A7720; A6570

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17. Stress and stress relaxation in integrated circuit metals and dielectrics
INS 91-24 4015570 B91076888 (EEA) NDN- 083-0401-5570-3

AUTHORS- Draper, B. L.; Hill, T. A.
JOURNAL NAME- Journal of Vacuum Science & Technology B (Microelectronics Processing and Phenomena)
ABBREVIATED JOURNAL TITLE- J. Vac. Sci. Technol. B, Microelectron. Process. Phenom. (USA)
VOLUME 9
NUMBER 4
PUBLICATION DATE- July-Aug. 1991
PP 1956-62
18 REFERENCES
DOCUMENT TYPE- Journal paper

ISSN- 0734-211X
CODEN- JVTBD9
CORPORATE AUTHOR- Sandia Nat. Labs., Albuquerque, NM, USA
COPYRIGHT CLEARANCE CENTER CODE- 0734-211X/91/041956-07$01.00
PUBLICATION COUNTRY- USA
LANGUAGE- English (DEF)
In order to provide data needed in the investigation and modeling of stress voiding in integrated circuit metallizations, stress and stress relaxation in Al/Si/Cu alloys and common dielectrics were studied as a function of storage temperature and deposition conditions. It was found that the room-temperature tensile stress in Al/Si/Cu increases with increasing substrate bias and deposition temperature, and that the isothermal relaxation rate upon cooling from 400 degrees C is sharply dependent on temperature. The activation energy for the relaxation process was found to be 0.39 eV above 130 degrees C and about 0.08 eV at lower temperatures. For insulating layers deposited with plasma-enhanced chemical-vapor deposition techniques, strong correlations were found among stress, density, hydrogen content, deposition temperature, and film composition (oxides, nitrides, and several intermediate oxynitrides), with the highest levels of compressive stress (near 1 GPa) being measured in nitride films deposited at 300 degrees C. These films, as well as phosphorus-doped glasses used as capping/protection layers, were found to undergo structural changes upon post-deposition thermal cycling which affected stress levels.

DESCRIPTOR- aluminium alloys; copper alloys; dielectric thin films; internal stresses; metallisation; plasma CVD coatings; silicon alloys; stress relaxation
IDENTIFIER- activation energy; capping/protection layers; compressive stress; deposition conditions; deposition temperature; integrated circuit metals; isothermal relaxation rate; metallizations; nitride films; plasma-enhanced chemical-vapor deposition techniques; post-deposition thermal cycling; room-temperature tensile stress; storage temperature; stress relaxation; stress voiding; substrate bias; AlSiCu; 0.08 to 0.39 eV
NUMERICAL DATA INDEXING- electron volt energy 8.0E-02 to 3.9E-01 eV
CHEMICAL INDEXING- AlSiCu/int Al/int Cu/int Si/int AlSiCu/ss Al/ss Cu/ss Si/ss
TREATMENT CODE- TC-P; TC-X
SECTIONAL CLASSIFICATION CODE- B2550F; B0520F; B2550E

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18. Properties of a photoimageable thin polyimide film
INS 91-22 4000730 B91067960 (EEA) NDN- 083-0400-0730-0

AUTHORS- Maw, T.; Hopla, R. E.
EDITOR- Lillie, E. D.; Ho, P. S.; Jaccodine, R.; Jackson, K.
ABBREVIATED JOURNAL TITLE- Electronic Packaging Materials Science V. Symposium
PUBLICATION DATE- 1991
PP 71-6
xiii+455 PAGES
5 REFERENCES
DOCUMENT TYPE- Conference paper
CORPORATE AUTHOR- Ciba-Geigy Corp., Ardsley, NY, USA
SPONSORING AGENCY- Mater. Res. Soc
PUBLISHER- Mater. Res. Soc
PUBLICATION PLACE- Pittsburgh, PA, USA

PUBLICATION COUNTRY- USA
CONFERENCE DATE- 26-29 Nov. 1990
CONFERENCE LOCATION- Boston, MA, USA
LANGUAGE- English (DEF)
Mechanical properties (tensile modulus, tensile strength, elongation at break), thermal properties (T/sub g/, CTE, thermo-decomposition temperature, and rate of weight loss) and electrical properties of Probimide 414 cured films have been determined. The mechanical properties of Probimide 414 thin films are highly dependent on the hard-bake temperature, hard-bake time and purge gas, but not dependent on the level of the exposure energy or the presence of 1% Irganox 1010 (w/w) as a stabilizer. At a hard-bake temperature of 350 degrees C and a nitrogen purge rate of 15 SCFH, Probimide 414 films showed excellent retention of the mechanical properties during extended heat treatment.
DESCRIPTOR- elongation; glass transition (polymers); heat treatment; integrated circuit technology; packaging; permittivity; polymer films; pyrolysis; tensile strength; thermal expansion
IDENTIFIER- dielectric constant; electrical properties; elongation; exposure energy; extended heat treatment; glass transition temperature; hard-bake temperature; hard-bake time; integrated circuits ; mechanical properties; packaging; photoimageable thin polyimide film; stabilizer; tensile modulus; tensile strength; thermal properties; thermo-decomposition temperature; weight loss rate; CTE; Irganox 1010; N/sub 2/ purge gas; Probimide 414 cured films; 0.5 to 14 hours; 15 SCFH films; 350 degC
NUMERICAL DATA INDEXING- temperature 6.23E+02 K; time 1.8E+03 to 5.0E+04 s

CHEMICAL INDEXING- N2/el N/el
TREATMENT CODE- TC-X
SECTIONAL CLASSIFICATION CODE- B0560; B0170J; B2810; B2570

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19. Control of thin film materials properties used in high density multichip interconnect
INS 90-04 3743142 B90069319 (EEA) NDN- 083-0374-3142-2

AUTHORS- Reche, J. J. H.
EDITOR- Jaccodine, R.; Jackson, K. A.; Lillie, E. D.; Sundahl, R. C.
ABBREVIATED JOURNAL TITLE- Electronic Packaging Materials Science IV. Symposium
PUBLICATION DATE- 1989
PP 39-46
xiii+494 PAGES
39 REFERENCES
DOCUMENT TYPE- Conference paper
CORPORATE AUTHOR- Polycon, Ventura, CA, USA
SPONSORING AGENCY- Army Res. Office; Allied-Signal Corp.; Amoco; Dow; Intel; Office Naval Res
PUBLISHER- Mater. Res. Soc
PUBLICATION PLACE- Pittsburgh, PA, USA
PUBLICATION COUNTRY- USA
CONFERENCE DATE- 24-28 April 1989
CONFERENCE LOCATION- San Diego, CA, USA
LANGUAGE- English (DEF)

Most literature on high density multichip interconnect (HDMI) focuses almost exclusively on processing of the organic dielectric. Nevertheless, it is only one of the components in high density multichip modules. Substrate properties, metal dielectric adhesion, internal stresses in the various films, and many other physico-chemical properties of the materials, can all be affected by neighbouring layers or process parameters improperly identified. Thus, in the course of process development, the real causes of difficulties and observed phenomenas can easily be misconstrued. The paper reviews some of the relationships between the properties of the thin film metallization and their effects on the dielectric layers. It also points out to some of the difficulties that can occur when treating the dielectric and the metallic layers as separate issues.
DESCRIPTOR- adhesion; integrated circuit technology; internal stresses; metallisation; packaging; polymer films; reviews
IDENTIFIER- adhesion; dielectric layers; high density multichip interconnect; high density multichip modules; internal stresses; metal dielectric adhesion; physico-chemical properties; polyimide film; process parameters; substrate properties; tensile stress; thin film material properties control; thin film metallization; HDMI
TREATMENT CODE- TC-G; TC-P
SECTIONAL CLASSIFICATION CODE- B2550F; B2570; B0170J

Citations from INSPEC (80-89): IN3

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20. Metalized MIC substrates using high K dielectric resonator materials
INS 89-01 3312580 B89015238 (EEA) NDN- 161-0331-2580-8

AUTHORS- Tamura, H.; Nishikawa, T.; Wakino, K.; Sudo, T.
JOURNAL NAME- Microwave Journal
ABBREVIATED JOURNAL TITLE- Microw. J. (USA)
VOLUME 31
NUMBER 10
PUBLICATION DATE- Oct. 1988
PP 117-18, 120, 122, 124, 126
3 REFERENCES
DOCUMENT TYPE- Journal paper
ISSN- 0026-2897
CODEN- MCWJAD
CORPORATE AUTHOR- Murata Manuf. Co. Ltd., Kyoto, Japan
PUBLICATION COUNTRY- USA
LANGUAGE- English (DEF)
The authors describe newly developed metallised substrates using high permittivity dielectric resonator materials. Their pore sizes were reduced to 2 mu m average and 5 mu m maximum so that they could be covered with high resolution circuit patterns. Compared with thin-film alumina substrates, they have the following advantages and disadvantages. The advantages are as follows: since they have higher dielectric constants, circuits utilizing electric length elements (such as stubs or filters) are miniaturized; and as they have a temperature coefficient of 0 p.p.m./ degrees C, temperature-stable microstrip line filters can be constructed directly on the substrate. The disadvantages are as follows: thermal conductivity of these materials is 10 times smaller than that of alumina; they have flexural strength 50 to 70

percent that of alumina; and they are expensive since they need surface polishing. Other characteristics (such as surface roughness, pore size and distribution, tensile strength between substrate and metallised electrode, and thickness of metallisation) are comparable to those of alumina substrates.
DESCRIPTOR- ceramics; dielectric materials; dielectric resonators; integrated circuit technology; metallisation; microwave integrated circuits ; substrates; thin film circuits
IDENTIFIER- ceramics; dielectric resonator materials; high permittivity; high resolution circuit patterns; high K; metallised substrates; microstrip line filters; microwave IC; pore sizes; thermal conductivity; thin film circuits; BaO; BaO-PbO-Nd/sub 2/O/sub 3/-TiO/sub 2/; MIC substrates; Nd/sub 2/O/sub 3/; PbO; TiO/sub 2/; ZrSnTiO/sub 4/; 2 to 5 micron
NUMERICAL DATA INDEXING- size 2.0E-06 to 5.0E-06 m
CHEMICAL INDEXING- ZrSnTiO4/ss O4/ss Sn/ss Ti/ss Zr/ss O/ss; BaOPbONd2O3TiO2/ss Nd2/ss Ba/ss Nd/ss O2/ss O3/ss Pb/ss Ti/ss O/ss; TiO2/bin O2/bin Ti/bin O/bin; BaO/bin Ba/bin O/bin; PbO/bin Pb/bin O/bin; Nd2O3/bin Nd2/bin Nd/bin O3/bin O/bin
TREATMENT CODE- TC-P
SECTIONAL CLASSIFICATION CODE- B1350F; B2220E; B2810; B2890; B0540

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21. Stresses in borophosphosilicate glass films during thermal cycling
INS 89-00 3279154 A88141344 (PHA); B89002629 (EEA) NDN- 161-0327-9154-3

AUTHORS- Townsend, P. H.; Huggins, R. A.
EDITOR- Rothman, L. B.; Herndon, T.
ABBREVIATED JOURNAL TITLE- Proceedings of the Symposium on Multilevel Metallization, Interconnection, and Contact Technologies
PUBLICATION DATE- 1987
PP 134-41
vii+272 PAGES
6 REFERENCES
DOCUMENT TYPE- Conference paper
CORPORATE AUTHOR- Dept. of Mater. Sci. & Eng., Stanford Univ., CA, USA
PUBLISHER- Electrochem. Soc
PUBLICATION PLACE- Pennington, NJ, USA
PUBLICATION COUNTRY- USA
CONFERENCE DATE- 21-22 Oct. 1986
CONFERENCE LOCATION- San Diego, CA, USA
LANGUAGE- English (DEF)
Stresses in thin films of borophosphosilicate glass deposited by atmospheric pressure CVD were measured during thermal cycling. Films of two different doping concentrations were examined for their flow properties. Initial heating produces an increase in the tensile stress as a consequence of film densification. Further heating leads to a decrease in the stress level as a result of plastic flow in the film. The addition of boron to PSG increases the tendency of the films to undergo plastic flow at elevated temperatures. Constant temperature flow behavior between 500 degrees C and 700 degrees C was nonlinear. The activation energy for plastic flow was found to be 150 kcal/mole (6.5 eV/particle).
DESCRIPTOR- borosilicate glasses; heat treatment; insulating thin films; metallisation; phosphosilicate glasses; plastic flow; thermal stresses; CVD coatings

IDENTIFIER- activation energy; atmospheric pressure CVD; constant temperature flow; doping concentrations; film densification; flow properties; glass films; heating; insulating dielectric layer; nonlinear behaviour; plastic flow; tensile stress; thermal cycling; BPSG; B2O3-P2O5-SiO2; IC metallisation; 500 to 700 degC
NUMERICAL DATA INDEXING- temperature 7.73E+02 to 9.73E+02 K
CHEMICAL INDEXING- B2O3-P2O5-SiO2/int B2O3/int P2O5/int SiO2/int B2/int O2/int O3/int O5/int P2/int Si/int B/int O/int P/int B2O3/bin P2O5/bin SiO2/bin B2/bin O2/bin O3/bin O5/bin P2/bin Si/bin B/bin O/bin P/bin
TREATMENT CODE- TC-X
SECTIONAL CLASSIFICATION CODE- A8140G; A6860; A8140L; A6220F; B2830E; B2550F; B2810 .

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22. Low stress films of cyclized polybutadiene dielectrics by vacuum annealing
INS 89-00 3279151 B89001989 (EEA) NDN- 161-0327-9151-9

AUTHORS- Salazar, M.; Wilkins, C. W., Jr.; Ryan, V. W.; Wang, T. T.
EDITOR- Rothman, L. B.; Herndon, T.
ABBREVIATED JOURNAL TITLE- Proceedings of the Symposium on Multilevel Metallization, Interconnection, and Contact Technologies
PUBLICATION DATE- 1987
PP 96-102
vii+272 PAGES
7 REFERENCES
DOCUMENT TYPE- Conference paper
CORPORATE AUTHOR- AT&T Bell Labs., Murray Hill, NJ, USA
PUBLISHER- Electrochem. Soc
PUBLICATION PLACE- Pennington, NJ, USA
PUBLICATION COUNTRY- USA
CONFERENCE DATE- 21-22 Oct. 1986
CONFERENCE LOCATION- San Diego, CA, USA
LANGUAGE- English (DEF)
The authors report a vacuum annealing technique for the post-deposition processing of cyclized polybutadiene dielectric (CBR) films. The technique has proven effective in reducing film stress from 3.1+or-0.5*10/sup 8/ dynes/cm/sup 2/ (tensile) to 1.4+or-0.2/sup 8/*10/sup 4/ dynes/cm/sup 2/ when the material is thermally cycled between 20 and 280 degrees C. For 10 mu m thick films the technique results in a net reduction in Si wafer bow by a factor of two. This reduction in wafer bow is important in the building of multilevel metallization structures where problems with patterning of films and automatic wafer handling equipment are encountered with excessively bowed substrates. A change in the glass transition temperature from approximately 320 to approximately 130 degrees C was also observed in the vacuum treated films and mechanical coupling to the substrate was seen to occur at approximately 175 degrees C instead of 280 degrees C.
DESCRIPTOR- annealing; dielectric thin films; integrated circuit technology; metallisation; polymer films
IDENTIFIER- cyclized polybutadiene dielectrics; film stress reduction; glass transition temperature; low stress polymer films; mechanical coupling; multilevel metallization structures; post-deposition processing; thermal cycling; vacuum annealing; vacuum treated films; IC technology; Si wafer bow reduction; 10 micron; 20 to 280 degC
NUMERICAL DATA INDEXING- temperature 2.93E+02 to 5.53E+02 K; size 1.0E-05 m

CHEMICAL INDEXING- Si/sur Si/el
TREATMENT CODE- TC-P; TC-X
SECTIONAL CLASSIFICATION CODE- B2550F; B2810; B2830C; B0560

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23. Passivation of GaAs FET's with PECVD silicon nitride films of different stress states
INS 88-04 3252065 B88071823 (EEA) NDN- 161-0325-2065-2

AUTHORS- Chang, E. Y.; Cibuzar, G. T.; Pande, K. P.
JOURNAL NAME- IEEE Transactions on Electron Devices
ABBREVIATED JOURNAL TITLE- IEEE Trans. Electron Devices (USA)
VOLUME 35
NUMBER 9
PUBLICATION DATE- Sept. 1988
PP 1412-18
12 REFERENCES
DOCUMENT TYPE- Journal paper
ISSN- 0018-9383
CODEN- IETDAI
CORPORATE AUTHOR- Unisys Corp., St. Paul, MN, USA
COPYRIGHT CLEARANCE CENTER CODE- 0018-9383/88/0900-1412$01.00
PUBLICATION COUNTRY- USA
LANGUAGE- English (DEF)
The passivation of GaAs MESFETs with plasma-enhanced chemical-vapor-deposited (PECVD) silicon nitride films of both compressive and tensile stress is reported. Elastic stresses included in GaAs following nitride passivation can produce piezoelectric charge density, which results in a shift of MESFET characteristics. The shift of MESFET parameters due to passivation was found to be dependent on gate orientation. The experiments show that nitride of tensile stress is preferable for MESFETS with (011-bar) oriented gates. The shifts in V/sub TH/,I/sub DSS/, and G/sub M/ of the devices before and after nitride passivation are less than 5% if the nitride of appropriate stress states are used for passivation. The breakdown voltage of the MESFETs after nitride deposition was also studied. It is found that the process with higher hydrogen incorporation tends to reduce the surface oxide and increase the breakdown voltage after nitride deposition. In addition, the passivation of double-channel HEMTs is reported for the first time.
DESCRIPTOR- dielectric thin films; electric breakdown of solids; field effect integrated circuits ; gallium arsenide; high electron mobility transistors; integrated circuit technology; microwave integrated circuits ; passivation; semiconductor technology; silicon compounds; stress effects; CVD coatings; III-V semiconductors; Schottky gate field effect transistors
IDENTIFIER- breakdown voltage; characteristics shift; compressive stress; double-channel HEMTs; elastic stresses; gate orientation; microwave IC; monolithic IC; nitride passivation; piezoelectric charge density; plasma-enhanced chemical-vapor-deposited; surface oxide reduction; tensile stress; CVD coating; GaAs; H incorporation; III-V semiconductors; MESFETs; MMIC; PECVD; Si/sub 3/N/sub 4/
CHEMICAL INDEXING- Si3N4/int Si3/int N4/int Si/int N/int Si3N4/bin Si3/bin N4/bin Si/bin N/bin; H/el; GaAs/int As/int Ga/int GaAs/bin As/bin Ga/bin
TREATMENT CODE- TC-X
SECTIONAL CLASSIFICATION CODE- B0520F; B1350F; B2550E; B2560S; B2570H

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24. Characterization of a spin-applied dielectric for use in multilevel metallization
INS 88-03 3213789 B88057504 (EEA) NDN- 161-0321-3789-5

AUTHORS- Riley, P. E.; Shelley, A.
JOURNAL NAME- Journal of the Electrochemical Society
ABBREVIATED JOURNAL TITLE- J. Electrochem. Soc. (USA)
VOLUME 135
NUMBER 5
PUBLICATION DATE- May 1988
PP 1207-10
25 REFERENCES
DOCUMENT TYPE- Journal paper
ISSN- 0013-4651
CODEN- JESOAN
CORPORATE AUTHOR- Fairchild Res. Center, Palo Alto, CA, USA
PUBLICATION COUNTRY- USA
LANGUAGE- English (DEF)
The spin-applied polysiloxane film Futurrex ICI-200 has been examined for use as a planarizing component of the dielectric layers of high density integrated circuits utilizing multiple levels of interconnecting metallization. The thickness of the as-spun film varies significantly with cure: it is invariant after thermal curing at 190 degrees C in vacuo or 250 degrees C in air and after additional curing at 450 degrees C in N/sub 2/ or Ar. However, the index of refraction decreases from 1.414 after curing at 190 degrees C to 1.340 after curing at 450 degrees C in either inert ambient. Treatment of the thermally cured films (190 degrees or 450 degrees C) with an O/sub 2/ plasma for 30 min in a barrel reactor results in a decrease in thickness of approximately 40% and a concomitant increase in the index of refraction from 1.414 to 1.438. Despite this large reduction in thickness, the stress of the film is low (1.7*10/sup 9/ dyn/cm/sup 2/, tensile) after O/sub 2/-plasma curing. Etch rates of the thermally and O/sub 2/-plasma cured films in HF and P-etch solutions suggest that the organosilicon material becomes porous and inorganic-like after exposure to the O/sub 2/ plasma in a barrel reactor. This is supported by the Fourier transform infrared (FTIR) spectra of the material; after curing in an O/sub 2/ plasma the band assigned to CH/sub 3/ substituents of the polysiloxane is absent, while a band at 1060 cm/sup -1/, which is close to the position of the Si-O-Si stretching vibration in SiO/sub 2/, sharpens and increases in intensity. In addition, although the FTIR spectra of the films cured at 190 degrees C in vacuo or at 450 degrees C in N/sub 2/ are featureless from 3100 to 3600 cm/sup -1/, that of the O/sub 2/-cured film exhibits a small, broad absorption in this region, suggestive of the presence of absorbed water or the formation by hydrolysis of Si-OH moieties in this apparently more porous framework.
DESCRIPTOR- dielectric thin films; infrared spectra of organic molecules and substances; integrated circuit technology; metallisation; polymer films; refractive index
IDENTIFIER- absorbed water; as-spun film; barrel reactor; dielectric; etch rates; high density integrated circuits ; hydrolysis; index of refraction; multilevel metallization; organosilicon material; planarization; polysiloxane; porous; stress; stretching vibration; thermal curing; thickness; Futurrex ICI-200; FTIR spectra; O/sub 2/ plasma
CHEMICAL INDEXING- O2/el O/el

TREATMENT CODE- TC-X
SECTIONAL CLASSIFICATION CODE- B2550F; B2570

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25. Material characteristics of spin-on glasses for interlayer dielectric applications
INS 88-01 3111185 A88044772 (PHA); B88026019 (EEA) NDN- 161-0311-1185-9

AUTHORS- Pei-lin Pai; Chetty, A.; Roat, R.; Cox, N.; Chiu Ting
JOURNAL NAME- Journal of the Electrochemical Society
ABBREVIATED JOURNAL TITLE- J. Electrochem. Soc. (USA)
VOLUME 134
NUMBER 11
PUBLICATION DATE- Nov. 1987
PP 2829-34
16 REFERENCES
DOCUMENT TYPE- Journal paper
ISSN- 0013-4651
CODEN- JESOAN
CORPORATE AUTHOR- Intel Corp., Components Res., Santa Clara, CA, USA
PUBLICATION COUNTRY- USA
LANGUAGE- English (DEF)
The material properties of several commercial spin-on glasses were investigated. Infrared spectrophotometry was used to study the annealing effects on the contents of hydroxyl and organic groups. Their concentrations are found to be sensitive to the annealing temperatures and annealing ambients. Both the room-temperature stress and the in situ stress during annealing were monitored. The measured stress levels of films on Si wafers are low (less than 10/sup 8/ Pa in tensile) compared to other deposited silicon dioxide films. Dielectric properties, including dielectric constants and dissipation factors, were also examined as a function of annealing conditions. A strong correlation between the dielectric properties and the OH content in the film was established. Of the two films studied most extensively, one showed significantly better dielectric properties following low-temperature (<600 degrees C) curing. Both are good dielectric films for VLSI interlayer dielectric applications if high-temperature annealings are allowed.
DESCRIPTOR- annealing; dielectric thin films; glass; infrared spectra of inorganic solids; internal stresses; permittivity; semiconductor technology
IDENTIFIER- annealing; curing; dielectric constants; dissipation factors; films; infrared spectrophotometry; spin-on glasses; stress; Si wafers; VLSI interlayer dielectric
CHEMICAL INDEXING- Si/sur Si/el
TREATMENT CODE- TC-X
SECTIONAL CLASSIFICATION CODE- A6140D; A6855; A7755; B0570; B2550; B2810

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26. Stress measurements on multilevel thin film dielectric layers used in Si integrated circuits
INS 86-03 2753176 A86112945 (PHA); B86063194 (EEA) NDN- 161-0275-3176-3

AUTHORS- Chen, Y. S.; Fatemi, H.
JOURNAL NAME- Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films)
ABBREVIATED JOURNAL TITLE- J. Vac. Sci. Technol. A, Vac. Surf. Films (USA)
pt.1
VOLUME 4
NUMBER 3
PUBLICATION DATE- May-June 1986
PP 645-9
10 REFERENCES
DOCUMENT TYPE- Conference paper
ISSN- 0734-2101
CODEN- JVTAD6
CORPORATE AUTHOR- Adv. Mater. Res. Group, Adv. Micro Devices Inc., Santa Clara, CA, USA
COPYRIGHT CLEARANCE CENTER CODE- 0734-2101/86/030645-05$01.00
PUBLICATION COUNTRY- USA
CONFERENCE DATE- 19-22 Nov. 1985
CONFERENCE TITLE- Proceedings of the 32nd National Symposium of the American Vacuum Society
CONFERENCE LOCATION- Houston, TX, USA
LANGUAGE- English (DEF)
Thin film induced stresses on a silicon substrate measured at room temperature, using a stress gauge wafer deflection setup. The thermal oxide was in high compressive stress due to CTE mismatch between oxide and Si substrate. As deposited PSG was in tensile stress decreasing in stress level with increasing P content. After densification, stress was reversed to the compressive mode with no significant reduction in stress for 8%-10% phosphorus content. As deposited poly-Si was in the high compressive mode. However, subsequent doping reduced the stress to one-half of 'as deposited' level and after annealing at 1000 degrees C the stress was further reduced. Cold sputtered aluminium metallization doped with 1% Si was found in the compressive mode, while hot sputtered copper doped Al metallization was under tension. Both films annealed at 450 degrees C hydrogen ambient exhibit reduced compressive and tensile levels, respectively. The CVD P-glass passivation was under low compression while plasma nitride was in high compressive stress. Most of these observations confirm previous reports. However, referenced results are confirmed and additional measurements are performed using a relatively new detection gauge system.
DESCRIPTOR- dielectric thin films; integrated circuit technology; internal stresses; passivation
IDENTIFIER- annealing; densification; doping; multilevel thin film dielectric layers; passivation; phosphosilicate glass; plasma nitride; poly-Si; polycrystalline Si; semiconductors; sputtered aluminium metallization; stress gauge wafer deflection setup; thermal oxide; thin film induced stresses; Al; Al-Cu; Al-Si; PSG; Si integrated circuits ; Si/sub 3/N/sub 4/; SiO/sub 2/
TREATMENT CODE- TC-X
SECTIONAL CLASSIFICATION CODE- A6860; B2550E; B2570

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27. Laser photolytic deposition of thin films
INS 83-03 2127483 A83103064 (PHA); B83053456 (EEA) NDN- 161-0212-

7483-2

AUTHORS- Boyer, P. K.; Moore, C. A.; Solanki, R.; Ritchie, W. K.; Roche, G. A.; Collins, G. J.
EDITOR- Osgood, R. M.; Brueck, S. R. J.; Schlossberg, H. R.
ABBREVIATED JOURNAL TITLE- Laser Diagnostics and Photochemical Processing for Semiconductor Devices. Proceedings of a Symposium
PUBLICATION DATE- 1983
PP 119-27
xiii+298 PAGES
8 REFERENCES
DOCUMENT TYPE- Conference paper
ISBN- 0 444 00782 2
CORPORATE AUTHOR- Dept. of Electrical Engng., Colorado State Univ., Fort Collins, CO, USA
SPONSORING AGENCY- Air Force Office Sci. Res
PUBLISHER- North-Holland
PUBLICATION PLACE- New York, NY, USA
PUBLICATION COUNTRY- USA
CONFERENCE DATE- Nov. 1982
CONFERENCE LOCATION- Boston, MA, USA
LANGUAGE- English (DEF)
An excimer laser is used to photochemically deposit thin films of silicon dioxide, silicon nitride, aluminium oxide, and zinc oxide at low temperatures (100-350 degrees C). Deposition rates in excess of 3000 AA/min and conformal coverage over vertical walled steps were demonstrated. The films exhibit low defect density and high breakdown voltage and have been characterized using IR spectrophotometry, AES, and C-V analysis. Device compatibility has been studied by using photodeposited films as interlayer dielectrics, diffusion masks, and passivation layers in production CMOS devices. Additionally, the authors have deposited metallic films of Al, Mo, W, and Cr over large (>5 cm/sup 2/) areas using UV photodissociation of trimethylaluminium and the refractory metal hexacarbonyls. Both shiny metallic films as well as black particulate films were obtained depending on the deposition geometry. The black films are shown to grow in columnar grains. The depositions were made at room temperature over pyrex and quartz plates as well as silicon wafers. The authors have examined the resistivity, adhesion, stress and step coverage of these films. The films exhibited resistivities at most approximately 20 times that of the bulk materials and tensile stress no higher than 7*10/sup 9/ dynes/cm/sup 2/.
DESCRIPTOR- alumina; aluminium; chemical vapour deposition; chromium; insulating thin films; laser beam applications; metallic thin films; molybdenum; silicon compounds; tungsten; zinc compounds
IDENTIFIER- adhesion; black particulate films; columnar grains; device compatibility; diffusion masks; high breakdown voltage; interlayer dielectrics; laser pyrolytic deposition; low defect density; metallic films; passivation layers; photochemically deposit; photodeposited films; production CMOS devices; resistivity; step coverage; stress; tensile stress; thin films; vertical walled steps; Al; Al/sub 2/O/sub 3/; AES; C-V analysis; Cr; IR spectrophotometry; Mo; Si/sub 3/N/sub 4/; SiO/sub 2/; UV photodissociation; W; ZnO
TREATMENT CODE- TC-P; TC-X
SECTIONAL CLASSIFICATION CODE- A6855; A8115H; B0520F; B2550F; B2550G; B4360

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28. Low temperature double-exposed polyimide/oxide dielectric for VLSI multilevel metal interconnection
INS 83-01 2017251 B83018518 (EEA) NDN- 161-0201-7251-6

AUTHORS- Wade, T. E.
JOURNAL NAME- IEEE Transactions on Components, Hybrids, and Manufacturing Technology
ABBREVIATED JOURNAL TITLE- IEEE Trans. Compon. Hybrids Manuf. Technol. (USA)

VOLUME CHMT-5
NUMBER 4
PUBLICATION DATE- 1982
PP 516-19
12 REFERENCES
DOCUMENT TYPE- Journal paper
ISSN- 0148-6411
CODEN- ITTEDR
CORPORATE AUTHOR- Microelectronics Res. Lab., Mississippi State Univ., Mississippi State, MS, USA
COPYRIGHT CLEARANCE CENTER CODE- 0148-6411/82/1200-0516$00.75
PUBLICATION COUNTRY- USA
LANGUAGE- English (DEF)
By use of a double-exposed (double-etch) low temperature polyimide/oxide process, the packing density for both first and second level metal interconnection can be improved by some 35 percent and 30 percent, respectively, in the vicinity of the via. Moreover, the complete interconnect process may be realized at temperatures below 300 degrees C. Since polyimide can be applied in thick layers having negligible (tensile) stress, a planar surface results and also parasitic lead capacitances may be considerably reduced. This process is also amenable to either wet chemical or dry plasma processing.
DESCRIPTOR- dielectric thin films; integrated circuit technology; large scale integration; polymer films
IDENTIFIER- double-exposed polyimide/oxide dielectric; dry plasma processing; interconnect process; packing density; parasitic lead capacitances; planar surface; via; wet chemical processing; VLSI multilevel metal interconnection
TREATMENT CODE- TC-A; TC-P
SECTIONAL CLASSIFICATION CODE- B2550E; B2570

Citations from INSPEC (69-79): IN4

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29. A switching plate with aluminium membrane crossings of conductors
INS 73-00 506162 B73016463 (EEA) NDN- 082-0050-6162-5

AUTHORS- Svechnikov, S. V.; Kobylyatskaya, M. F.; Kimarskii, V. I.; Kaufman, A. P.; Kuzovlev, Yu. I.; Cherepov, Ye. I.; Fomin, B. I.
JOURNAL NAME- Poluprovodnikovaya Tekhnika i Mikroelektronika
ABBREVIATED JOURNAL TITLE- Poluprovodn. Tekh. Mikroelektron. (Ukrainian SSR)

NUMBER 10
PUBLICATION DATE- 1972
PP 70-3
5 REFERENCES
DOCUMENT TYPE- Journal paper
ISSN- 0554-6222
CODEN- PTMUAC
PUBLICATION COUNTRY- Ukrainian SSR, USSR
LANGUAGE- Russian
Describes a switching plate for monocrystalline integrated circuits , possessing a large number of interconnections, crossings and contacting areas; it is made in a three-layer form, using only two metals, aluminium and vanadium. The crossings possess a two-layer dielectric insulation, the upper layer being a thin diaphragm, fixed in tension on two stops. The contacting areas facilitate the junctions with beam-lead integrated circuits In another form junctions are made by a reverse-crystal method using ultrasonic welding of aluminium with aluminium.
DESCRIPTOR- aluminium; conductors (electric); integrated circuits ; metallic thin films
IDENTIFIER- contacting areas; crossings; interconnections; monocrystalline integrated circuits ; switching plate; Al membrane crossings
TREATMENT CODE- TC-X
SECTIONAL CLASSIFICATION CODE- B2110; B2220; B2570

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30. Internal stresses and resistivity of low-voltage sputtered tungsten films (microelectronic cct. conductor)
INS 73-00 505840 A73024515 (PHA); B73016101 (EEA) NDN- 082-0050-5840-7

AUTHORS- Sun, R. C.; Tisone, T. C.; Cruzan, P. D.
JOURNAL NAME- Journal of Applied Physics
ABBREVIATED JOURNAL TITLE- J. Appl. Phys. (USA)
VOLUME 44
NUMBER 3
PUBLICATION DATE- March 1973
PP 1009-16
DOCUMENT TYPE- Journal paper
ISSN- 0021-8979
CODEN- JAPIAU
CORPORATE AUTHOR- Bell Telephone Labs., Allentown, PA, USA
PUBLICATION COUNTRY- USA
LANGUAGE- English (DEF)
The continuing development of microelectronic circuits toward greater complexity has stimulated interest in new materials and processes compatible with the currently known silicon device technology. Tungsten has been considered as the first-level conductor for a multilevel structure due to its relatively low electrical resistivity, its thermal expansion coefficient which matches fairly well to that of silicon, its demonstrated good adherence to the dielectrics of interest, and its ability to withstand high-temperature processing. The present work is a part of a study of the dependence of the properties of low-voltage triode sputtered tungsten films upon deposition parameters. The electrical resistivity was observed to increase with increasing deposition rate, decreasing film thickness, and decreasing substrate

temperature. The internal stress was determined by two X-ray methods and in general, depending upon the deposition conditions, tensile or compressive stresses of the order 10/sup 9/-10/sup 10/ dyn/cm/sup 2/ were observed.
DESCRIPTOR- integrated circuits ; internal stresses; metal-insulator-semiconductor structures; metallic thin films; resistance (electric); sputtering; tungsten
IDENTIFIER- compressive stresses; compressive stresses; conductor; dielectrics; electrical resistivity; electron microprobe; internal stresses; lattice parameter; low voltage sputtered W film; microelectronic circuits; microstructure; multilevel structure; resistivity; silicon device technology; substrate temperature; tensile stress; thermal expansion coefficient; two exposure technique; W film
TREATMENT CODE- TC-X
SECTIONAL CLASSIFICATION CODE- A7340Q; B2110; B2220; B2530F; B2570

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31. An evaluation of methods for passivating silicon integrated circuits
INS 72-01 392832 B72019249 (EEA) NDN- 082-0039-2832-0

AUTHORS- Jones, R. E., Jr.
JOURNAL NAME- Insulation/Circuits
ABBREVIATED JOURNAL TITLE- Insul./Circuits (USA)
VOLUME 18
NUMBER 4
PUBLICATION DATE- April 1972
PP 23-8
22 REFERENCES
DOCUMENT TYPE- Journal paper
ISSN- 0020-4544
CODEN- ISCUBF
CORPORATE AUTHOR- IBM Corp., San Jose, CA, USA
PUBLICATION COUNTRY- USA
LANGUAGE- English (DEF)
Emphasis is on the need for additional insulating layers on the surface to isolate lines of conductors which cross over on the way to output terminals. Criteria for film selection are outlined.
DESCRIPTOR- insulation; integrated circuits ; semiconductor materials
IDENTIFIER- adhesion; cracks; degradation; dielectric constant; etching; glass; grain structure; low ion mobility; n-type; p-type; passivating silicon integrated circuits ; pinholes; resistivity; stability; tensile stresses; transistor characteristics
TREATMENT CODE- TC-G
SECTIONAL CLASSIFICATION CODE- B2220; B2570

Citations from WORLD PATENT FULLTEXT: PC2

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32. MULTICHIP INTEGRATED CIRCUIT MODULE AND METHOD OF FABRICATION, - 1992017901/WO-A1/
PCN 1992-10-15 1992017901/WO-A1 NDN- 052-0140-0809-9

INVENTOR- EICHELBERGER, Charles, W.
DATE FILED- 1992-03-26
PUBLICATION NUMBER- 1992017901/WO-A1
DOCUMENT TYPE- A1
PUBLICATION DATE- 1992-10-15
INTERNATIONAL PATENT CLASS- H01L02156; *H01L02328; *H01L02302
PATENT REFERENCE- 62122258/JP-A; 63293965/JP-A; 4630096/JP-A; 4860166/US-A; 5049980/US-A; 5065282/US-A
PCT APPLICATION NUMBER- 09202623/US
PATENT APPLICATION PRIORITY- 676,937
PRIORITY COUNTRY CODE- US
PRIORITY DATE- 1991-03-27
APPLICANT- INTEGRATED SYSTEM ASSEMBLIES CORPORATION
PUBLICATION COUNTRY- WO
DESIGNATED COUNTRY- AT; AU; BE; CA; CH; DE; DK; ES; FR; GB; GR; IT; JP; KR; LU; MC; NL; SE
A multichip integrated circuit package comprises a substrate (12) having a flat upper surface to which is affixed one or more integrated circuit chips (14) having interconnection pads (22). A polymer encapsulant (18) completely surrounds the integrated circuit chips (14). The encapsulant is provided with a plurality of via openings therein to accommodate a layer of interconnection metallization (20). The metallization (20) serves to connect various chips (14) and chip pads (22) with the interconnection pads (22) disposed on the chips (14). In specific embodiments, the module is constructed to be repairable, have high I/O capability with optimal heat removal, have optimized speed, be capable of incorporating an assortment of components of various thicknesses and function, and be hermetically sealed with a high I/O count. Specific processing methods for each of the various module features are described herein, along with additional structural enhancements.
NO-DESCRIPTORS .

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33. EXTENDED INTEGRATION SEMICONDUCTOR STRUCTURE AND METHOD OF MAKING THE SAME, -1990009093/WO-A1/
PCN 1990-08-23 1990009093/WO-A1 NDN- 052-0124-5626-6

INVENTOR- JACOBS, Scott, Laurence
DATE FILED- 1990-01-10
PUBLICATION NUMBER- 1990009093/WO-A1
DOCUMENT TYPE- A1
PUBLICATION DATE- 1990-08-23
INTERNATIONAL PATENT CLASS- H04N00916
PATENT REFERENCE- 4743568/US-A; 4783695/US-A; 4890157/US-A
PCT APPLICATION NUMBER- 09000069/US
PATENT APPLICATION PRIORITY- 301,792
PRIORITY COUNTRY CODE- US
PRIORITY DATE- 1989-01-25
APPLICANT- POLYLITHICS, INC.
PUBLICATION COUNTRY- WO
DESIGNATED COUNTRY- AT; AU; BB; BE; BF; BG; BJ; BR; CA; CF; CG; CH; CM; DE; DK; ES; FI; FR; GA; GB; HU; IT; JP; KP; KR; LK; LU; MC; MG; ML; MR; MW; NL; NO; RO; SD; SE; SN; SU; TD; TG
A low cost, lightweight, fast, dense and reliable extended integration semiconductor

structure is provided by forming a thin film multilayer wiring decal (15) on a support substrate and aligning and attaching one or more integrated chips to the decal. A support ring (33) is attached to the decal surrounding the aligned and attached integrated substrate, and the substrate is removed. Reach-through vias connect the decal wiring to the chips.
NO-DESCRIPTORS .

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34. REDUCING STEREOLITHOGRAPHIC PART DISTORTION THROUGH ISOLATION OF STRESS, -1989010255/WO-A1/
PCN 1989-11-02 1989010255/WO-A1 NDN- 052-0120-6199-1

INVENTOR- SMALLEY, Dennis, Rollette
DATE FILED- 1989-04-17
PUBLICATION NUMBER- 1989010255/WO-A1
DOCUMENT TYPE- A1
PUBLICATION DATE- 1989-11-02
INTERNATIONAL PATENT CLASS- B29C06724; *G11C01302; *B32B00110
PATENT REFERENCE- 2775758/US-A; 4575330/US-A; 4752498/US-A; 4801477/US-A
PCT APPLICATION NUMBER- 08901560/US
PATENT APPLICATION PRIORITY- 183,015
PRIORITY COUNTRY CODE- US
PRIORITY DATE- 1988-04-18
APPLICANT- 3D SYSTEMS, INC.
PUBLICATION COUNTRY- WO
DESIGNATED COUNTRY- JP; KR
An improved stereolithography system for generating a three-dimensional object (30) by creating a cross-sectional pattern of the object to be formed at a selected surface (23) of a fluid medium (22) capable of altering its physical state in response to appropriate synergistic stimulation by impinging radiation, particle bombardment or chemical reaction, using information defining the object which is specially processed to reduce curl, stress, birdnesting and other distortions, the successive adjacent laminae (30a, 30b, 30c), representing corresponding successive adjacent cross-sections of the object, being automatically formed and integrated together to provide a step-wise laminar buildup of the desired object, whereby a three-dimensional object is formed and drawn from a substantially planar surface of the fluid medium during the forming process. Reducing stereolithographic distortion through isolation of stress is described.
NO-DESCRIPTORS .

Citations from US PATENT FULLTEXT: US2

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35. Method of forming patterned polyimide films
PAT 1995-11-28 05470693 NDN- 064-2592-7787-5

INVENTOR- Sachdev, Krishna G.; Whitaker, Joel R.; Ahmad, Umar M.

PATENT NUMBER- 05470693
PATENT APPLICATION NUMBER- 837505
DATE FILED- 1992-02-18
PATENT DATE- 1995-11-28
NUMBER OF CLAIMS- 23
EXEMPLARY CLAIM- 1
FIGURES- 13
ART OR GROUP UNIT- 157
PATENT CLASS- Invention (utility) patent
PATENT ASSIGNEE- International Business Machines Corporation
ASSIGNEE CITY- Armonk
ASSIGNEE STATE- NY
FIRM- Whitham, Curtis, Whitham & McGinn; Ahsan, Aziz M.
US PATENT CLASS- 430315000O
US CLASSIFICATION REFERENCE- X430317000; X430324000; X430329000; X430330000
INTERNATIONAL PATENT CLASS- 6G03F00726
PATENT REFERENCE- 4353778; 4411735; 4436583; 4690999; 4702792; 4869777; 5122439; 5153303
PATENT REFERENCED BY- 06159666; 06163957; 06293012; 06303230; 06348301; 06352817; 06479395; 06483193; 05609994; 05667922; 05688719; 05755947; 05805424; 05932799; 06611046; 06677209; 06737723; 06756653; 06770537; 06780721; 06781192; 06838764; 06872671; 06073482; 06890847; 06901217
PATENT ASSIGNEE- INTERNATIONAL BUSINESS MACHINES CORPORATION
ASSIGNEE ADDRESS- A CORP. OF NEW YORK ASSIGNEE CITY- AMRONK
ASSIGNEE STATE- NEW YORK
NEW CLASSIFICATION- 430315000O
CURRENT CLASSIFICATION REFERENCE- X257E21257; X257E21578; X430317000; X430324000; X430329000; X430330000

A method of producing patterned polyimide films using wet development of polyimide precursors through a photoresist mask is disclosed. Low thermal coefficient of expansion (TCE) polyimide patterns are formed by starting with a polyamic acid precursor, typically, that derived from 3,3 prime ,4,4 prime -biphenyltetracarboxylic acid dianhydride-p-phenylenediamine (BPDA-PDA). Polyimide patterns are generated with complete retention of the intrinsic properties of the polyimide backbone chemistry and formation of metallurgical patterns in low TCE polyimide dielectric.

EXEMPLARY CLAIMS- Claim- 1. A method of producing patterned low thermal coefficient of expansion polyimide films, comprising the steps of: applying a polyamic acid precursor layer onto a substrate wherein said polyamic acid precursor in said layer is capable of imidizing to form a polyimide which has a thermal coefficient of expansion approximately equal to said substrate and is selected from the group consisting of 3,3 prime ,4,4 prime -biphenyltetracarboxylic dianhydride-p-phenylenediamine, 3,3,4,4 prime -biphenyltetracarboxylic dianhydride-benzidine, pyromellitic dianhydride-p-phenylenediamine, pyromellitic dianhydride-benzidine, and 3,3 prime 4,4 prime -benzophenone tetracarboxylic acid dianhydride-p-phenylenediamine; partially baking said polyamic acid precursor layer to a point where a significant amount of casting solvent in said polyamic acid precursor layer has been removed but wherein said polyamic acid precursor layer is still subject to development; applying a positive photoresist on said polyamic acid precursor layer; imagewise exposing said positive photoresist to radiation through a mask; developing said positive photoresist with a first developer which is more active for said positive photoresist than for said polyamic acid precursor layer to yield a structure comprised of a patterned photoresist, a polyamic acid precursor layer and a

substrate, said step of developing is performed under conditions where said polyamic acid precursor layer is not etched with said first developer, said first developer being an aqueous developer; immersing said substrate in a second developer which is more active for said polyamic acid precursor layer than for said positive photoresist, said second developer being an aqueous developer; removing polyamic acid precursor material exposed to said second developer to produce a patterned polyamic acid precursor layer; and curing said patterned polyamic acid precursor layer to yield a patterned polyimide which has a low thermal coefficient of expansion.

NO-DESCRIPTORS .

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36. Global planarization process
PAT 1994-02-08 05284804 NDN- 064-2519-6676-4

INVENTOR- Moslehi, Mehrdad M.
PATENT NUMBER- 05284804
PATENT APPLICATION NUMBER- 816458
DATE FILED- 1991-12-31
PATENT DATE- 1994-02-08
NUMBER OF CLAIMS- 19
EXEMPLARY CLAIM- 1
FIGURES- 5
ART OR GROUP UNIT- 114
PATENT CLASS- Invention (utility) patent
PATENT ASSIGNEE- Texas Instruments Incorporated
ASSIGNEE CITY- Dallas
ASSIGNEE STATE- TX
FIRM- Garner, Jacqueline J.; Donaldson, Richard L.; Hiller, William E.
US PATENT CLASS- 437228000
US CLASSIFICATION REFERENCE- X216038000; X437195000; X437238000; X437240000; X437245000
INTERNATIONAL PATENT CLASS- 5H01L021461
PATENT REFERENCE- 4655874; 4676868; 4708770; 4732658; 4775550; 4810335; 4839311; 4962063; 4983545; 5079188; 5110763
PATENT REFERENCED BY- 05879862; 05885900; 05372974; 05532188; 05837603; 06690044; 06355553
PATENT ASSIGNEE- TEXAS INSTRUMENTS INCORPORATED, A DE CORP. ASSIGNEE ADDRESS- 13500 NORTH CENTRAL EXPRESSWAY ASSIGNEE CITY- DALLAS
ASSIGNEE STATE- TEXAS
NEW CLASSIFICATION- 438698000
CURRENT CLASSIFICATION REFERENCE- X216038000; X257E21027; X257E21243; X257E21304; X438010000; X438699000
A novel global planarization process is disclosed which is fully compatible with semiconductor processing. The process disclosed is called metal melt-solidification planarization (MMSP). A layer of a low melting point/high boiling point metal such as tin or a suitable alloy is deposited on a nonplanar wafer surface via physical-vapor deposition or chemical-vapor deposition or evaporation or plating. The wafer is then heated to above the tin melting point, cooled back to resolidify tin, and etched back to form a globally planar surface.
EXEMPLARY CLAIMS- Claim- 1. A method of planarizing a structure lying on a substrate comprising: depositing a disposable planarization layer which is in solid

form at room temperature; forming a liquid melt from said planarization layer over the substrate so as to form a planar liquid melt surface; solidifying said melt so as to form a planar solid layer; etching back said planar solid layer to a predetermined level on said structure.
NO-DESCRIPTORS .

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37. Avoiding spin-on-glass cracking in high aspect ratio cavities
PAT 1992-06-02 05119164 NDN- 064-2446-9512-4

INVENTOR- Sliwa, Jr., John W.; Dixit, Pankaj
PATENT NUMBER- 05119164
PATENT APPLICATION NUMBER- 652306
DATE FILED- 1991-02-05
PATENT DATE- 1992-06-02
NUMBER OF CLAIMS- 3
EXEMPLARY CLAIM- 1
FIGURES- 4
ART OR GROUP UNIT- 253
PATENT CLASS- Invention (utility) patent
PATENT ASSIGNEE- Advanced Micro Devices, Inc.
ASSIGNEE CITY- Sunnyvale
ASSIGNEE STATE- CA
FIRM- Benman & Collins
US PATENT CLASS- 2577760000
US CLASSIFICATION REFERENCE- X357071000
INTERNATIONAL PATENT CLASS- 5H01L02934; H01L02348; H01L02946
PATENT REFERENCED BY- 05250472; 05382547; 05393709; 05516720; 05517062; 05661049; 05665632; 05668398; 05716888; 05773361; 05936295; 06025260; 06031286; 06132814; 06136687; 06576976; 06607991; 06734564; 06228744; 06232647; 06251799; 06307265; 06306753
FOREIGN DOCUMENT REFERENCE- 58-4947; 60-49649; 61-160953
FOREIGN COUNTRY CODE- JPX; JPX; JPX
NEW CLASSIFICATION- 2577760000
CURRENT CLASSIFICATION REFERENCE- X257E21581; X257E23142; X257E23144; X257E23167
Before spin-on-glass (SOG) is applied and soft-cured over metal traces (10) having a height/width aspect ratio (of the spaces) of at least 1, the aluminum metal traces are selectively coated with selective tungsten (16). After SOG (18) is spun on and soft-cured, it is etched back to expose the metal interconnects. A selective tungsten wet etch in H sub 2O sub 2 detaches the SOG from the metal walls, leaving silt-like voids (20). Stress-free SOG hard curing may now proceed. A capping layer (22) of SOG may now be applied, soft-cured, then hard-cured. Alternatively, other dielectric materials may be applied as the capping layer. Further, interfacial lateral sidewall voids (24) may be deliberately left unfilled, by employing a capping layer (24 prime) of vapor-deposited oxide. The unfilled voids have a dielectric constant of 1.0, which is useful in extremely high speed devices. The resulting structure is comparatively stress-free as fabricated and is resistant to later environmentally-induced brittle tensile fracture.
EXEMPLARY CLAIMS- Claim- 1. An integrated circuit containing a plurality of low-resistivity metal interconnect layers in which at least two of said adjacent layers are electrically isolated and separated from each other by a cavity having a height H and

a width W and occupied by a first layer of a dielectric material consisting essentially of spin-on-glass partially detached from adjacent interconnect sidewalls and by a second layer of a dielectric material which covers the top of said interconnects and fills at least a portion of a region between said first layer and said sidewalls, leaving a region of closed space located interfacially on said sidewalls, said region having a dielectric constant approximately equal to 1, thereby permitting use of cavities having an aspect ratio of H/W of at least about 1 between said interconnects.
NO-DESCRIPTORS .

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38. Method for coplanar integration of semiconductor ic devices
PAT 1991-02-05 04990462 NDN- 064-2405-8655-8

INVENTOR- Sliwa, Jr., John W.
PATENT NUMBER- 04990462
PATENT APPLICATION NUMBER- 337223
DATE FILED- 1989-04-12
PATENT DATE- 1991-02-05
NUMBER OF CLAIMS- 42
EXEMPLARY CLAIM- 1
FIGURES- 40
ART OR GROUP UNIT- 114
PATENT CLASS- Invention (utility) patent
PATENT ASSIGNEE- Advanced Micro Devices, Inc.
ASSIGNEE CITY- Sunnyvale
ASSIGNEE STATE- CA
FIRM- Collins, David W.
US PATENT CLASS- 437051000
US CLASSIFICATION REFERENCE- X148DIG028; X257661000; X257730000; X257776000; X437208000; X437226000
INTERNATIONAL PATENT CLASS- 5H01L021304
PATENT REFERENCE- 3301716; 3870850; 4154998; 4322737; 4542397; 4668333; 4858072
PATENT REFERENCED BY- 05102818; 05189595; 05198385; 05233500; 05283107; 05304460; 05395645; 05473513; 05498575; 05545291; 05565705; 05605863; 05648684; 05691248; 05706176; 05783856; 05808330; 05824186; 05834843; 05904545; 05909052; 05925924; 05968150; 06030885; 06150670; 06251219; 06543087; 06559956; 06611050; 06653157; 06687987; 06761302; 06864570; 06287949; 06300149; 06351022; 06348388; 06369445; 06379998; 06440775; 06455945; 06505665; 06890836
PATENT ASSIGNEE- ADVANCED MICRO DEVICES, INC., 901 THOMPSON ROAD, SUNNYVALE, CA 94088, A CORP. OF DE
NEW CLASSIFICATION- 438107000
CURRENT CLASSIFICATION REFERENCE- X029834000; X029836000; X148DIG028; X257661000; X257730000; X257776000; X257E21705; X257E23141; X257E23170; X257E25012; X257E29022
A high degree of wafer-scale integration of normally incompatible IC devices is achieved by providing a plurality of segments (10), each segment having thereon one or more circuits, circuit elements, sensors and/or I/O connections (14 prime). Each segment is provided with at least one edge (12) having an abutting portion (12a) capable of abutting against a similar edge of a neighboring segment. The segments are placed on the surface of a flotation liquid (20) and are allowed to be

pulled together so as to mate abutting edges of neighboring segments, thereby forming superchips (10 prime). Microbridges (22) are formed between neighboring segments, such as by solidifying the flotation liquid, and interconnections (26) are formed between neighboring segments. In this manner, coplanar integration of semiconductor ICs is obtained, permitting mixed and normally incompatible circuit functions on one pseudomonolithic device as diverse as silicon and III-V digital circuits, III-V optoelectonic devices, static RAMs, charge coupled devices, III-V lasers, superconducting thin films, ferromagnetic non-volatile memories, high electron mobility transistors, and bubble memories, to name a few, to be integrated in any desired combination. The yieldable scale of integration of a given device technology is also greatly extended. The segments are brought together in a particulate-free fashion with high throughput and exacting reproducibility at low cost.

EXEMPLARY CLAIMS- Claim- 1. A method for coplanar integration of semiconductor IC devices comprising: (a) providing segments having at least one edge having an abutting portion capable of abutting against a similar edge of a neighboring segment, each segment having on a top surface thereof at least one of the items selected from the group consisting of circuits, circuit elements, sensors, and input/output connections; (b) arranging said segments on the surface of a flotation liquid such that the top surfaces of each segment are substantially coplanar; (c) allowing said segments to be pulled together so as to mate abutting edges of neighboring segments to form a superchip; (d) forming solid microbridges between neighboring segments to mechanically secure said superchip; and (e) forming electrical interconnections between neighboring segments so as to interconnect various of said circuits, circuit elements, sensors, and input/output connections.
NO-DESCRIPTORS .

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39. Electro-optic signal measurement
PAT 1990-05-22 04928058 NDN- 064-2381-4169-7

INVENTOR- Williamson, Steven
PATENT NUMBER- 04928058
PATENT APPLICATION NUMBER- 355514
DATE FILED- 1989-05-23
PATENT DATE- 1990-05-22
NUMBER OF CLAIMS- 23
EXEMPLARY CLAIM- 1
FIGURES- 4
ART OR GROUP UNIT- 267
PATENT CLASS- Invention (utility) patent
PATENT ASSIGNEE- The University of Rochester
ASSIGNEE CITY- Rochester
ASSIGNEE STATE- NY
FIRM- LuKacher, Martin
US PATENT CLASS- 3240960000
US CLASSIFICATION REFERENCE- X359257000
INTERNATIONAL PATENT CLASS- 5G01R02914
PATENT REFERENCE- 4446426; 4603293; 4618449; 4618819; 4790635; 4836633
PATENT REFERENCED BY- 05041783; 05208531; 05434698; 05550370; 05592101; 05952818; 06111416; 06573700; 06587258; 06677769; 06388454; 06400165; 06414473; 06906506

PATENT ASSIGNEE- UNIVERSITY OF ROCHESTER, THE, A NOT-FOR-PROFIT CORP.

NEW CLASSIFICATION- 324096000O
CURRENT CLASSIFICATION REFERENCE- X359257000
Electro-optic probes which are adapted to be placed in the fringe field from electrical signals propagating on conductors (which may be conductors of an integrated circuit) and which modulate optical pulses passing therethrough, for example by modulating the polarization of the light in accordance with the Pockels effect, utilize thin bodies of electro-optic material, such as a single crystal of GaAs in a manner to reduce physical damage to the probe and to the circuit and to precisely locate the probe in the field of the signal being measured, such as adjacent to the conductor of interest. The electro-optic material that is used may also be implanted with high energy ions of low Z materials (e.g. hydrogen or oxygen) so as to create charge trapping sites and to reduce the photo conductivity of the semiconductive electro-optic material sufficiently that the dielectric relaxation time (where photo current through the material reduces by 1/e) is less than the duration of the optical pulses without eliminating the electro-optic (e.g. Pockels) effect.
EXEMPLARY CLAIMS- Claim- 1. In a system for electro-optically measuring an electrical signal which produces a field with an electro-optic element through which said field passes and through which an optical signal also passes and is modulated by said field, said measurement being in accordance with the modulation of said optical signal, an improved probe which comprises a support having a surface with an edge, a strip of flexural material mounted on said surface and extending beyond said edge as a cantilever, said cantilever having a free end, said electro-optical element being mounted on said element between said edge and said free end and extending beyond said free end to a region where said optical signal intersects said element whereby said element is flexurally supported.
NO-DESCRIPTORS .

Citations from US PATENT FULLTEXT: US3

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40. Formation and planarization of silicon-on-insulator structures
PAT 1986-08-05 04604162 NDN- 067-2264-7934-2

INVENTOR- Sobczak, Zbigniew P.
PATENT NUMBER- 04604162
PATENT APPLICATION NUMBER- 812531
DATE FILED- 1985-12-23
PATENT DATE- 1986-08-05
NUMBER OF CLAIMS- 11
EXEMPLARY CLAIM- 1
FIGURES- 8
ART OR GROUP UNIT- 131
PATENT CLASS- Invention (utility) patent
PATENT ASSIGNEE- NCR Corporation
ASSIGNEE CITY- Dayton
ASSIGNEE STATE- OH
FIRM- Cavender, J. T.; Salys, Casimer K.
US PATENT CLASS- 156657100O

US CLASSIFICATION REFERENCE- X156643100; X156649100; X156653100; X156662100; X427308000; X427337000; X427399000; X427407100; X437062000

INTERNATIONAL PATENT CLASS- H01L021308; H01L021312; H01L021318
PATENT REFERENCE- 4025411; 4307180; 4333965; 4361600; 4374011; 4377438; 4407851; 4485551; 4502913; 4561932; 4571819; 4580331
PATENT REFERENCED BY- 04676868; 04814287; 04842675; 04910165; 04923563; 04983545; 05084419; 05110755; 05116460; 05262002; 05458734; 05466621; 05635411; 05691230; 05721174; 05858547; 05892707; 05907170; 05907783; 05909618; 05914511; 05915192; 05936274; 05963469; 05963789; 05973356; 05976930; 05991225; 06004835; 06025225; 06043527; 06046477; 06066869; 06072209; 06093623; 06104061; 06110798; 06124729; 06134175; 06143636; 06150687; 06153468; 06156604; 06156607; 06165836; 06171972; 06174784; 06190950; 06190960; 06191448; 06191470; 06194262; 06194289; 06208164; 06215145; 06225147; 06238976; 06242775; 06246083; 06251752; 06255171; 06266268; 06300204; 06304483; 06306703; 06309950; 06317357; 06528837; 06538330; 06537871; 06552435; 06559032; 06589851; 06597037; 06610566; 06624021; 06630713; 06680240; 06680864; 06689660; 06747305; 06756622; 06764901; 06777744; 06784076; 06798009; 06812516; 06818937; 06852167; 06858504; 06861311; 06881627; 06884687; 06344399; 06348366; 06350635; 06362043; 06362070; 06373138; 06381168; 06399979; 06403429; 06417040; 06418050; 06423613; 06429065; 06434041; 06449186; 06455391; 06465298; 06465865; 06476434; 06477080; 06479370; 06486703; 06486027; 06492233; 06498065; 06509213; 06504201; 06515510; 06890812; 06894532; 06903367
PATENT ASSIGNEE- HYUNDAI ELECTRONICS AMERICA ASSIGNEE ADDRESS- 3101 NORTH FIRST STREET ASSIGNEE CITY- SAN JOSE ASSIGNEE STATE- CALIFORNIA
NEW CLASSIFICATION- 438410000O
CURRENT CLASSIFICATION REFERENCE- X257E21245; X257E21564; X427308000; X427337000; X427399000; X427407100; X438425000; X438699000
A process for fabricating silicon-on-insulator structures on semiconductor wafers and planarizing the topology of the patterns formed from the silicon. In the composite, the process provides for the formation of monocrystalline silicon islands electrically isolated by dielectric in substantially coplanar arrangement with surrounding dielectric. According to one practice of the process, substrate silicon islands are initially formed and capped, and thereafter used as masks to direct the anisotropic etch of the silicon substrate to regions between the islands. During the oxidation which follows, the capped and effectively elevated silicon islands are electrically isolated from the substrate by lateral oxidation through the silicon walls exposed during the preceding etch step. The capped regions, however, remain substantially unaffected during the oxidation. With the electrically isolated silicon island in place, a silicon dioxide layer and a planarizing polymer layer are deposited over the wafer. Processing is concluded with a pair of etching operations, the first removing polymer and silicon dioxide at substantially identical rates, and the second removing silicon dioxide and monocrystalline silicon at substantially identical rates.
EXEMPLARY CLAIMS- Claim- 1. A process for fabricating planarized silicon insulator structures on a semiconductor wafer, comprising the steps of: ; etching a monocrystalline silicon substrate to form islands of silicon having defined perimeters; ; capping the tops and sides of the silicon islands with oxidation masks; ; anisotropically etching deeper into the monocrystalline silicon substrate between the capped island and with no material undercut of the capped islands to increase the relative height of the islands; ; oxidizing the lateral walls of silicon formed by the anisotropic etch until the capped silicon is electrically isolated from the silicon substrate; ; depositing a dielectric layer to a thickness greater than the height of the

islands; ; forming a planarized polymer layer over the dielectric layers; ; simultaneously etching the polymer and dielectric layers to remove polymer and dielectric material at substantially equal rates until the polymer layer is absent; and ; simultaneously etching the dielectric layer and the electrically isolated silicon to remove dielectric material and silicon at substantially equal rates.
NO-DESCRIPTORS .

Citations from US PATENT FULLTEXT: US5

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41. Incorporation of dielectric layers in a semiconductor
PAT 1992-05-05 05110712 NDN- 196-2443-9436-3

INVENTOR- Kessler, Daniel D.; Wu, Robert W.; Beatty, Christopher C.; Crook, Mark D.
PATENT NUMBER- 05110712
PATENT APPLICATION NUMBER- 547093
DATE FILED- 1990-04-25
PATENT DATE- 1992-05-05
NUMBER OF CLAIMS- 9
EXEMPLARY CLAIM- 1
FIGURES- 5
ART OR GROUP UNIT- 156
PATENT CLASS- Invention (utility) patent
PATENT ASSIGNEE- Hewlett-Packard Company
ASSIGNEE CITY- Palo Alto
ASSIGNEE STATE- CA
FIRM- Cochran, II, William W.
US PATENT CLASS- 430312000
US CLASSIFICATION REFERENCE- X216051000; X216058000; X216066000; X427096000; X427099000; X430313000; X430314000; X430316000; X430317000; X437228000
INTERNATIONAL PATENT CLASS- 5G03C00500
PATENT REFERENCE- 4367119; 4447824; 4495220; 4539222; 4745045
PATENT REFERENCED BY- 05169802; 05244837; 05410185; 05565384; 05593921; 05818110; 05847457; 05912188; 05935766; 06027995; 06052261; 06054384; 06080529; 06117764; 06133141; 06143476
FOREIGN DOCUMENT REFERENCE- EP-A-O-046 525; 158884
FOREIGN COUNTRY CODE- EPX; JPX
A system for integrating a composite dielectric layer in an integrated circuit to facilitate fabrication of a high density multi-level interconnect with external contacts. The composite dielectric layer comprises of a polymer layer which normally comprises a polyimide that is deposited using conventional spin-deposit techniques to form a planarized surface for deposition of an inorganic layer typically comprising silicon dioxide or silicon nitride. The inorganic layer is etched using standard photoresist techniques to form an inorganic mask for etching the polymer layer. A previously deposited inorganic layer functions as an etch stop to allow long over etches to achieve full external contacts which, in turn, allows high density interconnect systems on multiple levels.
EXEMPLARY CLAIMS- Claim- 1. A process for forming a composite dielectric sandwich

in an integrated circuit through the use of inorganic dielectric layers comprising the steps of: (a) forming a first inorganic dielectric layer over at least one underlying layer of said integrated circuit that has sufficient strength to protect said underlying layer by distributing stress from subsequently formed metal features that are deposited on said first inorganic dielectric layer; (b) forming first metal features on said first inorganic dielectric layer; (c) forming a polymer layer over said first inorganic dielectric layer and said first metal features of said integrated circuit , said polymer layer being substantially uniformly distributed to provide a substantially planarized surface; (d) depositing a second inorganic dielectric layer in said integrated circuit over said polymer layer that provides sufficient strength to protect said polymer layer by distributing stress from subsequently formed second metal features that are deposited on said second inorganic dielectric layer; (e) forming a mask on said second inorganic dielectric layer; (f) etching said second inorganic dielectric layer using said mask as a masking pattern to form an inorganic dielectric mask and to provide a protective layer for etching of any subsequently deposited polymer layers; (g) etching said polymer layer using said inorganic dielectric mask as a masking pattern to essentially remove all polymer unmasked by said inorganic dielectric mask between said inorganic dielectric mask and said first inorganic dielectric layer such that said first inorganic dielectric layer functions as a protective layer and etch stop for said underlying layers wherever said etching of said polymer layer continues after all of said unmasked polymer has been removed to fully expose any existing external contact surfaces of said first metal features; (h) maintaining said second inorganic dielectric layer as an insulating layer that, together with said polymer layer, forms said composite dielectric sandwich that has sufficient strength to distribute stress from subsequently formed second metal features and that remains in said integrated circuit as an etch stop layer for subsequently formed layers in a multilayer integrated circuit ; (i) forming said second metal features on said second inorganic dielectric layer an in vias formed by etching said polymer layer.
NO-DESCRIPTORS .

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